Intl J Engg Sci Adv Research 2016 Dec;2(4):1-4 ISSN NO: 2395-0730

Design low power SRAM using MTCMOS Technique with Nanometer Regime

Ankita Tiwari
M.Tech Scholar
Rama University
Kanpur India
ankitaforfrndz@gmail.com

Raghvendra Singh
Assistant Professor, ECE Deptt.
RAMA University
Kanpur, India
Raghav.raghvendra7@gmail.com

***Abstract*— In this paper proposed to new high performance SRAM Cell with the help of MTCMOS Techniques. This paper represents the simulation of 6T SRAM cells using low power reduction techniques and their comparative analysis on different parameters such as Power Supply Voltage, Delay, Operating Temperature and the leakage power , leakage current and active power. In comparison to the conventional 6T SRAM bit-cell, the total leakage power is reduced. In all simulation have been carried out "Empyrean Aether" tool using 180 nm technologies.**

Keywords—read stability, write stability, MT CMOS techniques, SRAM and VLSI.

I. INTRODUCTION

In recent year, due to the demanding of high speed ,in VLSI field time to time improving the technologies in this field. here leakage power reduction is the major problem in CMOS technology. Minimizing power dissipation is therefore important, both for increasing levels of integration and to improve reliability, feasibility and cost[1]. SRam is basically used for the cache memory in microprocessor, main frame computers, engineering work places and memory puposes due to the high speed and low power consumption. IN 6T SRAM structure each bit is an SRAM is stored on four transitors thet form two cross coupled inverters. MTCMOS is an effective circuit level technique that provides a high performance and low-power design by utilizing both low and high-threshold voltage transistor [2]. In nano scale technology SRAM becomes inceasingly vulnerable to noise sources. For demanding low power consumption during active operation, The major role of supply voltage which is useful. The reliability of SRAM is depends on the low supply voltages. In this paper , We will emphasize SRAM read and write margin analysis and compare the different SRAM cells configuration on the basis of stability. For reducing the leakage component we have uses the threshold transistors. So we have designing the 6T SRAM cell. This cell is reducing power and fast operation. SRAM is a volatile memory which is used in microprocessor and ICS fabrication. Memory is important feature for reducing power such as RAM, ROM, Static RAM, Dynamic RAM, PROM, EEPROM several memory but RAM is used for low power and low voltage demand dur to recent year when ever Lap top, cell phones arises.

II. CONVENTIONAL 6T SRAM CELL

6T SRAM cell can be designed by using 2 PMOS and 4 NMOS transistor as shown in fig (a). It consist of two cross coupled inverters and two acess NMOS transistor M5 and M6 . These two cross coupled inverters, which are connected bach to back, are used for storing one bit of information at a time (either 0 or 1). The two additional acess transistor is used to control access to a storage cell during read and write operation. this access two enable by the word line (WL) which control these two access transistor M5 and M6 which, in turn , control weather the cell should be connected to the bit lines, bit and bit bar[10]. They are used to transfer data for both read and write operations. The value of bit and bit bar is inverted . when bit is high then bit bar will be zero and vice versa. widely used as criteria of stability. SNM is basically minimum DC noise voltages with the help of flip cell state. MT CMOS is an important technique for power dissipation. It is basically works on the high speed and reducing the leakage power. The SRAM to operate in read mode should have "readability" and "write stability" respectively.[3][4]. Power dissipation can be reduced by scaling the supply voltages. Which is most concernable issues in CMOS technique

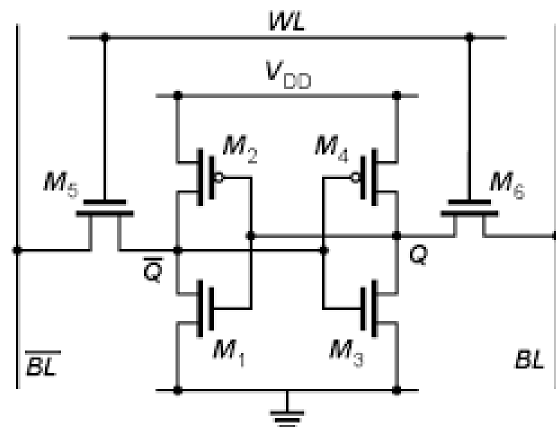

Fig (a) Schematic Diagram of 6T SRAM Cell

III. 6T SRAM CELL

The 6T SRAM cell can be designed with the help of PMOS and NMOS transistors. PMOS has two transistors and NMOS has a four transistors.shown in fig a. according to fig two cross coupled inverters and two access NMOS transistors M5 and M6 . These two cross coupled invereters, which is connected back to back , are used for storing 1 bit of information at a time (either 0 or 1) . the two additional acess transistor for storage cell during read and write operation. This access to the cell is enabled by word line (WL) which controls these two access cell should be connected to the bit lines, bit and bit bar [10]. They value of bit and bit bar is inverted . when bit is high then bit bar will be zero and vice versa.

- Here PMOS and NMOS both are used in cross coupled phenomena.

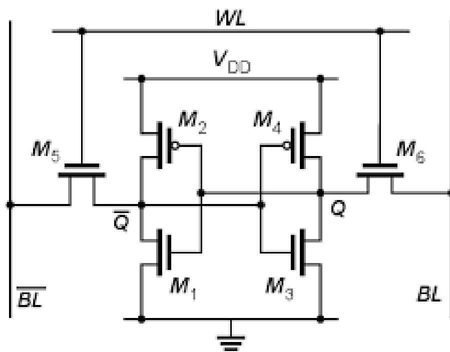

Fig b Schematic Diagram of 6T SRAM Cell

Three modes of operation is enrgised is as following

- Standby mode
- Read mode
- Write mode

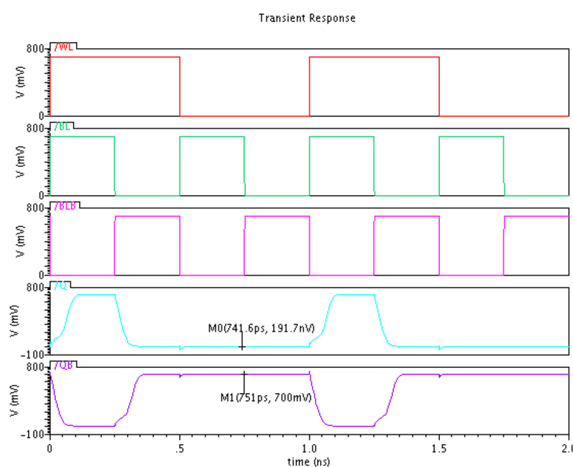

Fig. (c) output wave form of 6T SRAM cell

IV. MT CMOS TECHNIQUE

- In CMOS scaling the supply and threshold voltages is reduces. At low threshold voltages the leakage current is higher and the leakage power is higher. And so much energy is dissipated with the help of leakage current. Transistors which will be use is diminishing during the period. NOW the popular low leakage circuit is the Multithreshold voltage CMOS (MTCMOS).
- The multi threshold CMOS technology has two features, which is "active" and "sleep". these two features is tmportant of MTCMOS. In small leakage power dissipation it is so usefull.one side it is efficent power management and second side it two different threshold voltages are used for N channel and P channel MOSFET in a single chip [5]. this technique based on disconnecting the low threshold voltages (low –vt) logic gates from power supply and the ground line via a cut off high threshold voltages(high vt) sleep transistors is known as "power gatting". These technique as shown in fig (d) The schematic of power gating technique using MTCMOS is shown in Fig. 7.The transistors having low threshold voltage are used to implement the logic. The transistors having high threshold voltage are used to isolate.Power Gating Technique using MTCMOS. the low threshold voltage transistors from supply and ground during standby (sleep) mode to prevent leakage dissipation [6].

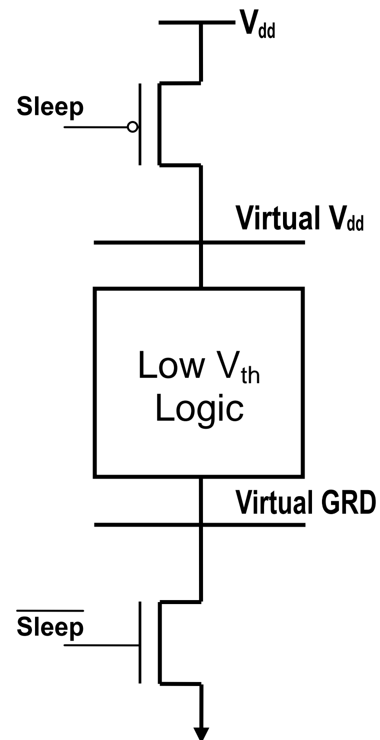

Fig. (d) MT CMOS Technique.

V. Modified SRAM Cell

Using multi threshold technique, The main purpose for reducing power we have to modified SRAM cell. According to the fig (c)

modified PMOS and NMOS in virtual Vdd and ground. In MT CMOS Techniques is used basically for power gatting and reduce leakage current. In modification of 6T SRAM cell supply voltage vdd where WL is adjusted adding PMOS and in ground pull down in sleep mode adding NMOS. according to fig (c)

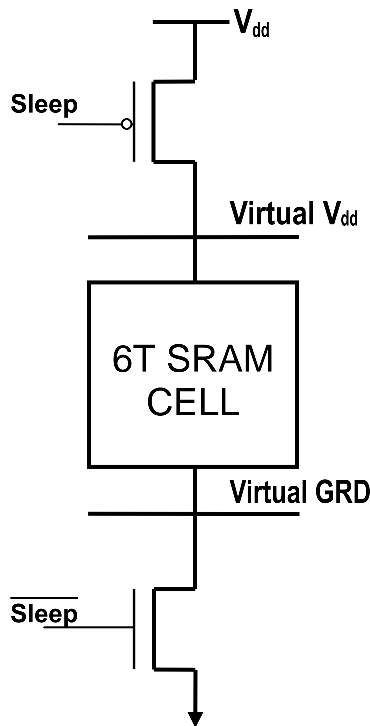

Fig. (e) Modified SRAM cell with MT CMOS

VI. Performance Analysis And Result Simulation

In this paper, We have performed simulation of our base 6T SRAM CELL and modified 6T SRAM CELL using MT CMOS technique on empyrean aether tool and SPECTRE simulator at 180nm technology.

A. *ACTIVE POWER*

Supply	Base 6T SRAM CELL		Modified 6T SRAM cell	
Supply and temperature	0.7V	27^{0}C	0.7V	27^{0}C
Active power (N w)	3.58	3.58	1.35	1.35

Active power dissipated by the circuit at operation condition. Here we will calculate active power at 180nm technology. The active power includes both dynamic and static power. The active power consumption of CMOS circuit [7][8] is described by following equation-

$$Pactive=Pdyanamic+Pstatic \quad (1)$$

$$= Pswitch+Pshort+Pleak \quad (2)$$

$$P=\alpha_{D-1} X\ C_l\ X\ F_{clock}\ X\ V^2_{dd} + I_{short\text{-}circuit}\ X\ V_{dd} + I_{leakage}\ X\ V_{dd} \quad (3)$$

Where α_{D-1} =Probability, C_l=Load capacitance, F_c=clock frequency, V_{dd} =Power supply, I_{short} =Short circuit current, I_{leak}= Leakage current. As shown in table here we will modified 6T SRAM cell using MT CMOS Technique.

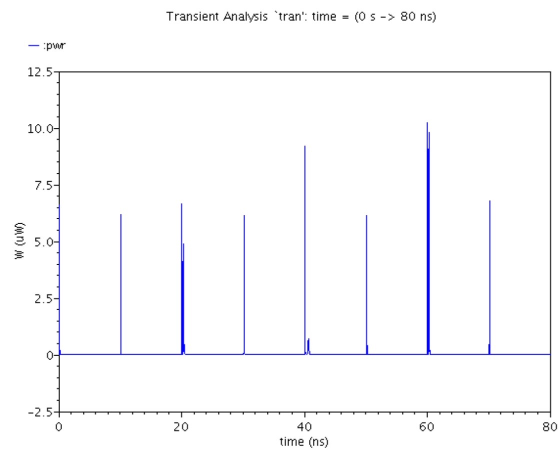

Fig. (f) Active power of 6T SRAM cell

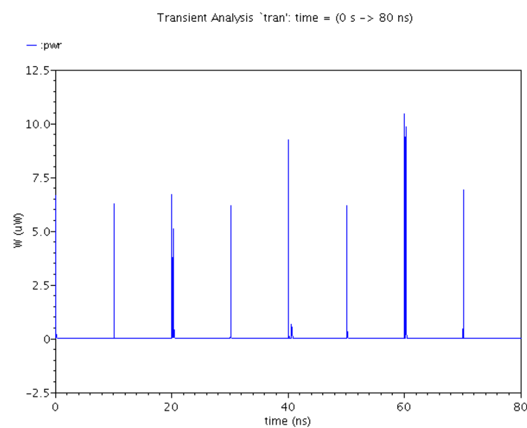

Fig (g) Active power of Modified 6T SRAM cell

Table 2 : Active power dissipation of 6T SRAM cell

Circuit	Base 6T	Modified 6T

	SRAM cell		SRAM cell	
Supply and Temperature	0.7 V	27° C	0.7 V	27°C
Active power (nW)	3.58	3.58	1.35	1.35

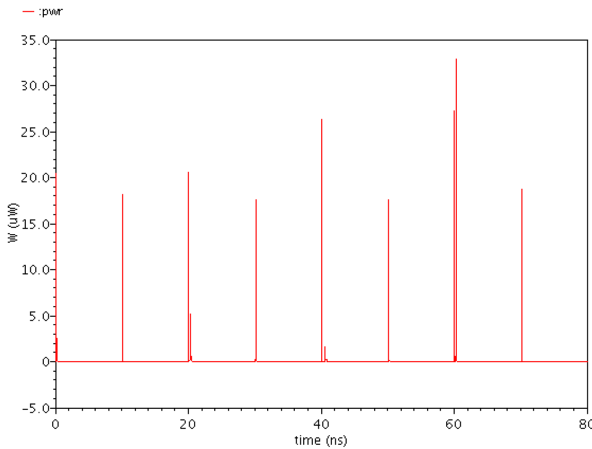

Fig (h) Active power dissipation of 6T SRAM cell

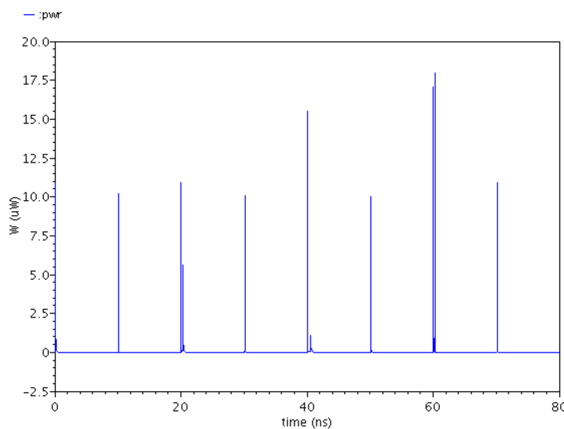

Fig (i) Active power dissipation of Modified 6T SRAM

B. STAND BY LEAKAGE CURRENT

This current operate when the cicuit is in idle mode. Here we connect the sleep transistor to the pull down network NMOS And to pull up network PMOS circuit. We measure the leakage current and power gatting using MT CMOS technique. The basic equation of leakage current is[9]

$$I_{Leakage}=I_{Sub}+I_{OX} \quad (4)$$

Where, I_{sub}=Sub threshold leakage current.

I_{ox} = Gate oxide current.

$$I_{Sub}= K_1We^{-vth/nvo}\ (1-e^{-v/vo}) \quad (5)$$

Where k1 and n is experimentally derived,W is gate width,Vθ is thermal voltage, n slope shape factor/ sub threshold swing coefficient,V_{th} is threshold voltage.

$$I_{ox}=K_2W(V/Tox)^2e^{-\alpha Tox/Vo} \quad (6)$$

Where K_2 and α are experimentally derived, Tox is oxide thickness. Stand by leakage current is measure. 7V voltage and 27°C temp. It is greatly 90% power gatting with modified 6T SRAM CELL using MT CMOS. In table 3 and 4. As shown various voltages and temperature.

- Table 3. STAND BY LEAKAGE CURRENT AND LEAKAGE POWER DUE TO VARIOUS VOLTAGES.

Voltage v	Leakage current		Leakage power	
	Base6T SRAM(n A)	Modified 6T SRAM (n A)	Base6T SRAM(n W)	Modified 6T SRAM (n W)
0.5	0.92	1.31	4.99	4.15
0.7	4.38	1.86	16.68	11.61
0.9	10.37.75	4.87	32.39	17.76
1.1	17.6	11.59	56.75	34.85
1.3	25.8	19.43	84.73	45.98

- Table 4. STAND BY LEAKAGE CURRENT AND LEAKAGE POWER DUE TO VARIOUS TEMPERATURE.

Temp. oC	Leakage current		Leakage power	
	Base 6T (nA)	Modi. 6T (pA)	Base 6T (nA)	Modi. 6T (pA)
27	4.38	1.86	16.68	11.61
47	4.46	1.92	17.43	12.68
67	4.60	2.02	18.19	13.77
87	4.84	2.16	18.91	14.09
107	4.91	2.30	19.63	14.56

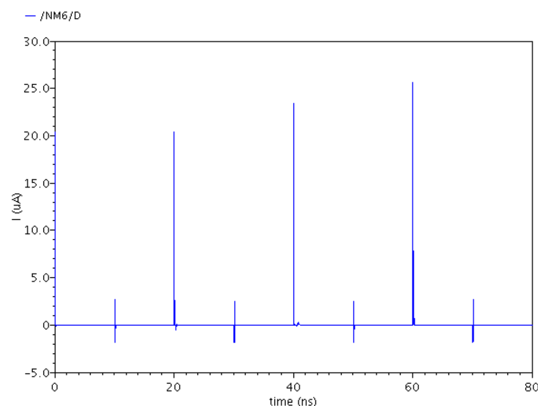

Fig (j) Stand by leakage current of 6T SRAM cell

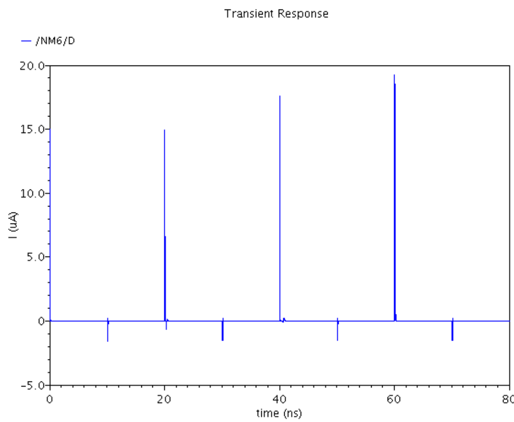

Fig (k) Stand by leakage current of Modified 6T SRAM cell

C. Stand by leakage power-

Stand by leakage power is measured at the time of idle mode. Leakege power is measured when the sleep transistor is off. The equation of leakage power is

$$P_{leakage}=I_{leakage}\, X\, V_{dd} \qquad (7)$$

Where P_{leak}=Leakage power,$I_{leakage}$=Leakage current and V_{dd} is supply voltage. According to the equation the power depends upon the leakage current and supply voltage.

- Table 3. STAND BY LEAKAGE POWER AND LEAKAGE CURRENT DUE TO VARIOUS TEMPERATURE.

Temp in 0C	Leakage current		Leakage power	
	base 6T SRAM (nA)	modified 6T SRAM (nA)	base 6T SRAM (nW)	modified 6T SRAM(nW)
27	4.38	1.86	16.68	11.61
47	4.46	1.92	17.43	12.68
67	4.60	2.02	18.19	13.77
87	4.84	2.16	18.91	14.09
107	4.91	2.30	19.63	14.56

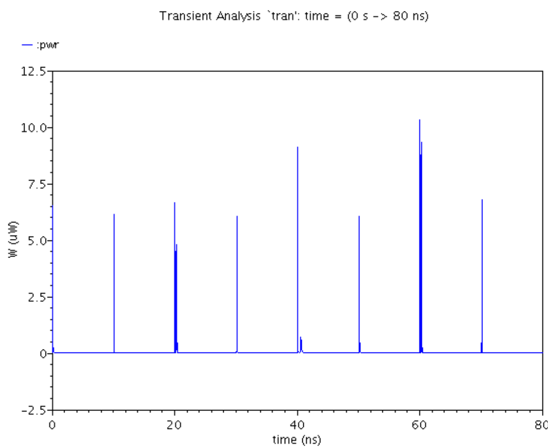

Fig (l) stand by leakage power of 6T SRAM cell

CONCLUSION

The Simulation result discussed above improve the read and write stability of SRAM which is increased the power dissipation and due to increase in area.The Stability performances of three SRAM cell topologies have been presented. As process technologies continue to advance, the speed of SRAMs will increase, but devices will be more susceptible to mismatches, which worsen the static-noise margin of SRAM cells. MTCMOS technique in power dissipation which is improving the stability and performance of CMOS circuit.

ACKNOWLEDGEMENTS

The authors wish to thank the Management, Dean-FET and the Head of Electronics & Communication Engineering of Mody Institute of Technology & Science (Deemed University)

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