Static Noise Margin Analysis of Low Power SRAM Cell for High Speed Application

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***Abstract*—Low power design is the industry buzzword these days in present chip design technologies. CMOS technology continues to drive the reduction in switching delay and power while improving area density. However, the transistor miniaturization also introduces many new challenges in Very Large Integrated (VLSI) circuit design, such as sensitivity to process variations, increasing transistor leakage and reducing Static Noise Margin. This paper is focused on the different types of analysis applied on noise, voltage, read and write margin of Static Random Access Memory (SRAM) cell for high-speed application and to get an appropriate Static Noise Margin (SNM). The analysis is performed on Cadence virtuoso tool, gpdk 180nm technology.**

Keywords— Static Noise Margin, SRAM, VLSI, CMOS

I. INTRODUCTION

This paper introduces how the speed of the SRAM cell depends on the different types of noise analysis. Both cell ratio and pull-up ratio are important parameters because these are the only parameters in the hand of the design engineer [1]. Technology is getting more complex day by day. Presently in industry, 32 nm CMOS process technology is used. So it should be carefully selected in the design of the memory cell. There are number of design criteria that must be taken into the consideration.

The two basic criteria which we have taken such as –

Data read operation should not be destructive.

Static noise margin should be in the acceptable range [2].For demand of the high speed SRAM cell operation, supply voltage scaling is often used. Therefore, the analysis of SRAM read/write margin is essential for high speed SRAMs.

A key insight of this paper is that we analyze different types of noise margin for high speed SRAM cell. We evaluate the different SNM curves with respect to Noise Margin, Data Retention Voltage, Read and Write Margin. At the end we conclude that how these above parameters affect SNM and speed of the SRAM cell.

After Simulation and considering all these parameters, we find an appropriate value of SNM.

II. STATIC NOISE MARGIN

In this section, first we introduce existing static approach that is butterfly method for measuring static noise margin [1]. Static noise margin of the SRAM cell depends on the cell ratio (CR), supply voltage and pull up ratio. For stability of the SRAM cell good SNM is required. Driver transistor is responsible for 70 % value of the SNM [3].

Cell ratio is the ratio between sizes of the driver transistor to the load transistor during the read operation [1]. Pull up ratio is the ratio between sizes of the load transistor to the access transistor during write operation [1]. The basic circuit of SRAM cell is shown in given below as figure 1and 4.

CR= (W1/L1) / (W5/L5) (During Read Operation)
PR = (W4/L4) / (W6/L6) (During Write Operation)

SNM, which affects both read margin and write margin, is related to the threshold voltages of the NMOS and PMOS devices in SRAM cells [3]. Typically, to increase the SNM, the threshold voltages of the NMOS and PMOS devices need to be increased. However, the increase in threshold voltage of PMOS and NMOS devices is limited. The reason is that SRAM cells with MOS devices having high threshold voltages are difficult to operate; as it is hard to flip the operation of MOS device.

Changing the cell ratio, we get different speeds of SRAM cell. If cell ratio increases, then size of the driver transistor also increases, hence current also increases. As current increases, the speed of the SRAM cell also increases. By changing the cell ratio we get corresponding SNM. This is same for DRV vs. SNM.

Finally butterfly structure is obtained as shown in Fig.5. Since by knowing the diagonals of the maximum embedded squares we can calculate the sides. The squares have maximum size when the lengths of their diagonal D1 and D2 are maximum; the extremes of this curve correspond to the diagonals of the maximum embedded.

The DC response of Standard 6T SRAM is shown in Figure 2. The DC response is showing Supply Voltage (VDD), Output Voltage (VOUT), and current on its respective nodes. The DC Response is also showing the Input Power and Output Power, clearly indicating that the output q and qb are compliment to each other. The layout of standard 6T SRAM cell is shown in Figure 3.

III. DATA RETENTION VOLTAGE

Data Retention Voltage (Vdr): Min. power supply voltage to retain high node data in the standby mode [1]. There are two nodes (q and qb) of the SRAM cell for storing value either 0 or 1. Then decrease the power supply voltage until the flip the state of SRAM cell or content of the SRAM cell remain

constant. Vdd scales down to DRV, the Voltage Transfer Curves (VTC) of the internal inverters degrade to such a level that Static Noise Margin (SNM) of the SRAM cell reduces to zero.

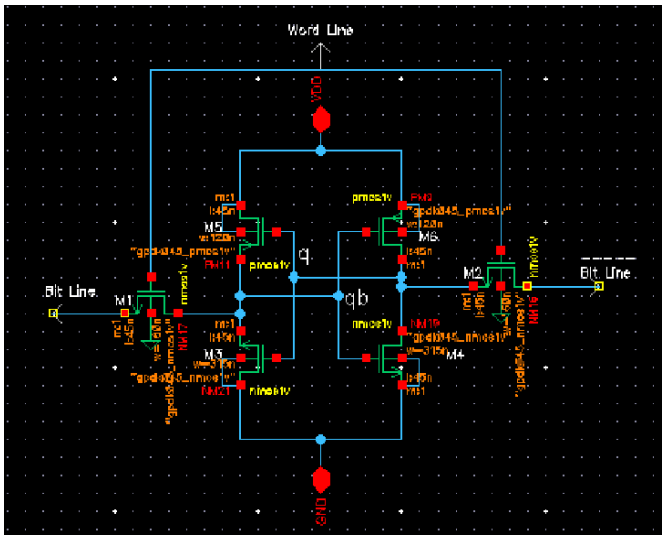

Fig.1. Schematic Diagram for basic SRAM cell.

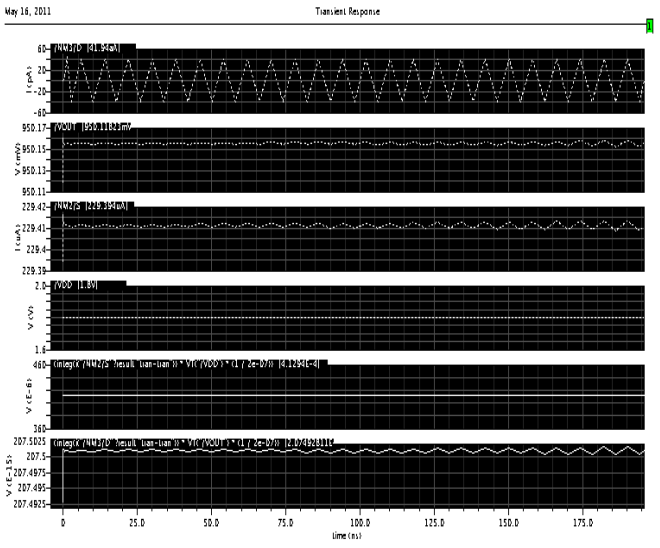

Fig.2. Transient Response of 6T SRAM

If Q=1, Q'=0, it is changes the value of Q=0, Q'=1 after decreasing the value of the power supply voltage. Data retention voltage should be greater than threshold voltage. We took the value of power supply voltage upto 0.6V then it is change the state of cell. We know, minimum power supply voltage to retain high node data in the standby mode: Vdr = Vdd = 0.6V for 180 nm Technology that is data retention voltage.

IV. WRITE MARGIN

Write margin is defined as the minimum bit line voltage required toflip the state of an SRAM cell [1]. The write margin value and variation is a function of the cell design, SRAM array size and process variation.

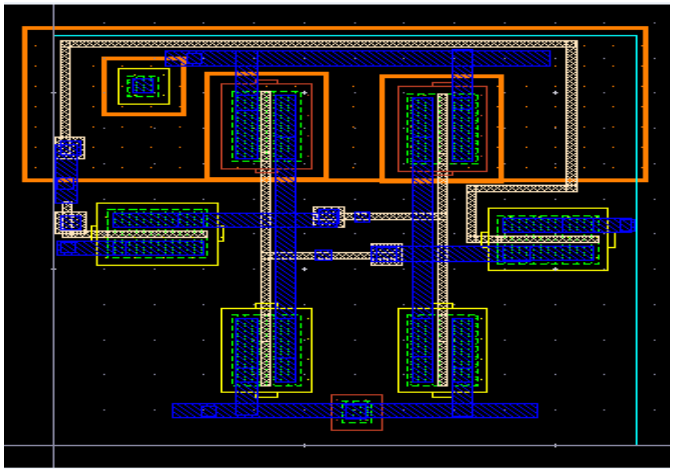

Fig.3. Layout of Standard 6T SRAM

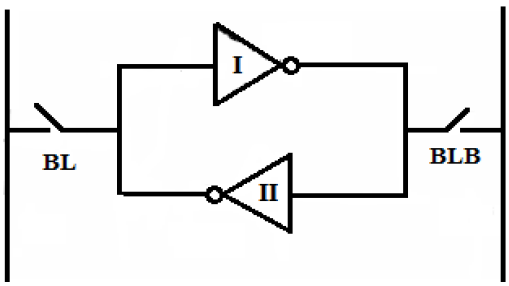

Fig.4. Circuit for two cross couple inverter with BL and BLB [1].

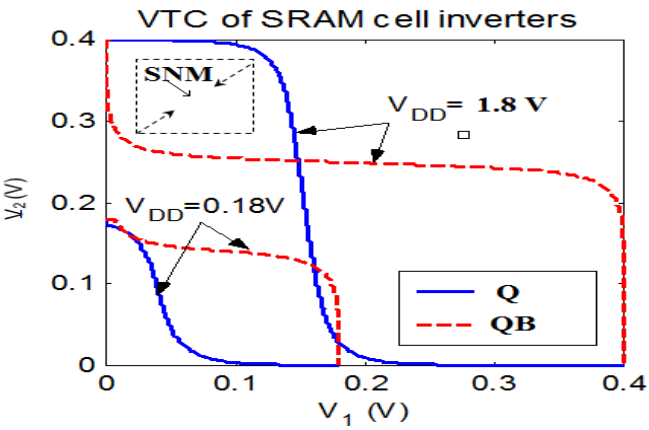

Fig.5. Circuit for the calculation of SNM after rotation [1].

Already five existing static approaches for measuring write margin are available [5]. First we calculated write margin by the existing bl sweeping method then we compared that with Static Noise Margin.

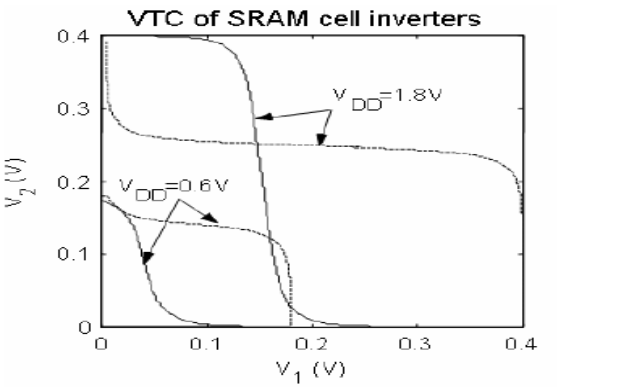

Fig. 6. VTC of SRAM cell during DRV calculation.

Write margin is directly proportional to the pull up ratio. Write margin increases with the increases value of the pull up ratio.[6] So carefully you have to design SRAM cell inverters before calculating the write margin of SRAM cell during write operation. Pull up ratio also fully depends on the size of the transistor. RM shown in figure 7.

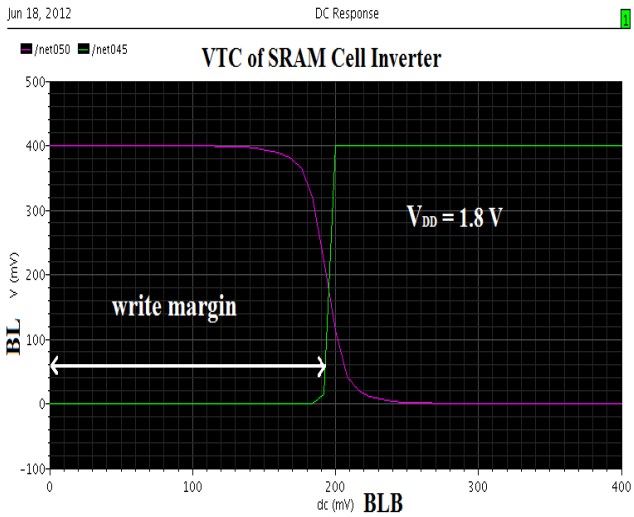

Fig.7. VTC of SRAM cell to get write margin calculation by the BL sweeping method.

V. READ MARGIN

Based on the VTCs, we define the read margin to characterize the SRAM cell's read stability. We calculate the read margin based on the transistor's current model [7-10]. Experimental results show that the read margin accurately captures the SRAM's read stability as a function of the transistor's threshold voltage and the power supply voltage variations. Below figure 9 shows the read margin of the SRAM cell during read operation.

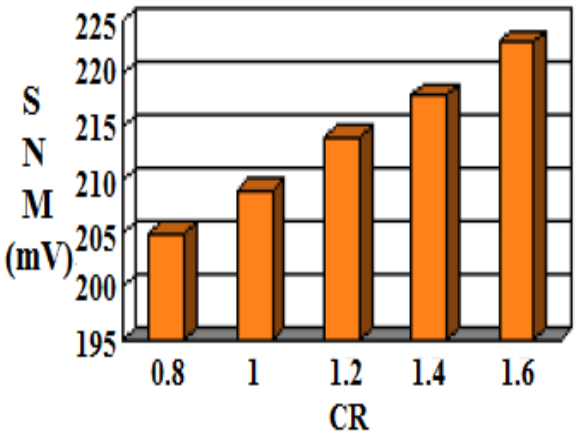

Fig.8. The graphical representation of CR vs. SNM of the SRAM cell.

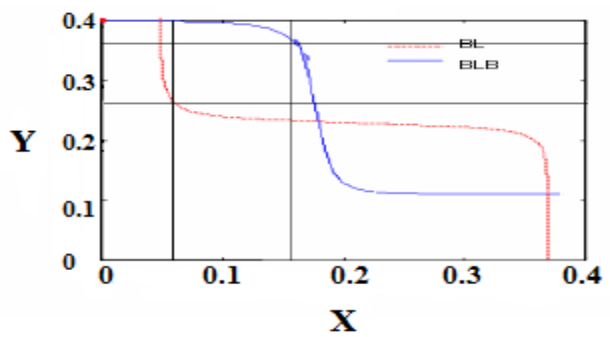

Fig.9. Shows the read margin.

Read margin is directly proportional to the cell ratio. Read margin increases with the increase in value of the pull up ratio. So carefully you have to design SRAM cell inverters before calculating the read margin of SRAM cell during read operation. Pull up ratio also fully depends on the size of the transistor. The process of analysis of read margin is same as the analysis of static noise margin.[11-16]

VI. SIMULATION RESULTS AND DISCUSSION

Some important results that are observed from simulation of the schematic designed in S-Edit are summarized below:
The cell ratio and the pull up ratio of the SRAM cell are given below:
CR= (W1/L1) / (W5/L5) =1(During Read Operation)
PR = (W4/L4) / (W6/L6) =3 (During Write Operation)
The range cell ratio and pull-up ratio should be in 1-2.5 and 3-4 respectively otherwise data will be destroy.
SNM calculation: We have done the SNM calculation by this way with respect of above figure:
Side of the Maximum Square =A=0.209V=209 mV,

Lengths of diagonal of Square (D) = √ 2 * One side of the Square

= √ 2 * 209,

SNM = D/ √ 2 = √ 2 * 209/√ 2,

So SNM =One of the side=A=209 mV.

If W/L ratio of driver transistor increases, Cell Ratio also increases which increases the Static noise margin, current driving capability and speed of the SRAM Cell. The Graph 8 shows that when SNM increases, CR increases. CR increases means the size of driver transistor increases.

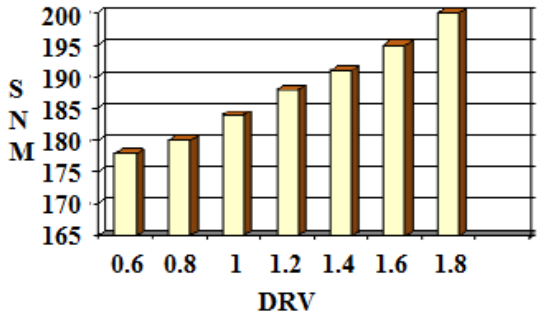

Fig.10. The graphical representation of DRV vs. SNM of the SRAM cell.

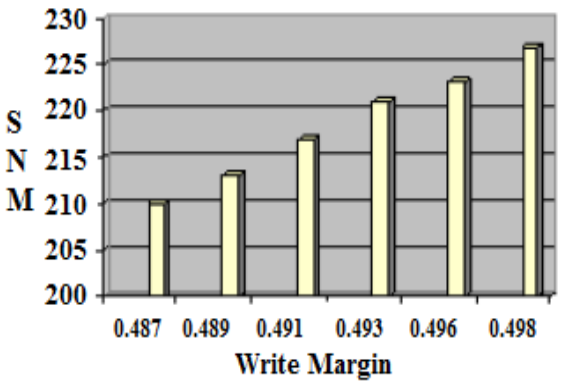

Fig.11. The graphical representation of Write Margin vs. SNM of the SRAM cell

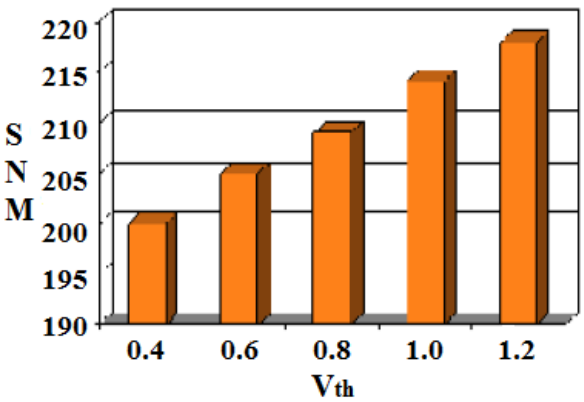

Fig.12. The graphical representation of threshold voltage vs. SNM of the SRAM cell

TABLE I. CR VS. SNM

Technology	CR	SNM (mV)
180 nm	0.8	205
	1.0	209
	1.2	214
	1.4	218
	1.6	223

TABLE II. DRV VS. **SNM**

Technology	DRV (V)	SNM (mV)
180nm	1.8	200
	1.6	195
	1.4	191
	1.2	188
	1.0	184
	0.8	180
	0.6	178

TABLE III. WRITE MARGIN VS. SNM

Technology	PR	Write	SNM(mV)
180 nm	3.0	0.487	210
	3.2	0.489	213
	3.2	0.491	217
	3.6	0.493	221
	3.8	0.496	223
	4.0	0.498	227

TABLE IV. THRESHOLD VOLTAGE VS. SNM

Technology	Threshold	SNM
180nm	PMOS: -	200
	PMOS: -	205
	PMOS: -	209
	PMOS: -	214

	PMOS: -	218

Data Retention Voltage also affects SNM of the SRAM cell and it is an important parameter to reduce supply voltage shown in Table I. Data Retention Voltage should be greater than threshold voltage i.e. 0.6V which is shown in Table II the Graph 10 shows that SNM increases when DRV increases. If DRV is reduced and kept above threshold voltage, the contents of the SRAM cell will not be affected.

The Graph 11 shows SNM increases when read margin increases and read margin increases means the read operation of the SRAM cell is optimized. Table III shows the write margin vs. SNM. We observe that both write margin and SNM are proportional with respect to the PR.

The graph 11 shows SNM increases when write margin increases. Write margin increases means the write operation of the SRAM cell is optimized. Table IV shows the threshold voltage vs. SNM. We observe that if the threshold voltage increases the value of the SNM also increases.

The graph 12 shows SNM increases when threshold voltage increases.

VII. CONCLUSION

In this paper, we have analyzed Static Noise Margin with parameters such as Data Retention Voltage, Write Margin, Read Margin and Threshold voltage during read/write operation. We have analyzed read margin and write margin for read and write ability as Static Noise Margin affects both read margin and write margin. Read margin and write margin also depends on pull up ratio and cell ratio respectively. The range of cell ratio and pull-up ratio should be 1 to 2.5. The W/L ratio of load transistor should be 3-4 times greater than the access transistor.

This paper is based on the reliability of SRAM circuits and systems. We have considered four major parameters SNM, DRV, RM and WM of SRAM cell. We have reduced supply voltage using Data Retention Voltage Technique and an appropriate SNM is obtained.

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REFERENCES

[1] Andrei Pavlov & Manoj Sachdev, "CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies". Intel Corporation, University of Waterloo, 2008 Springer Science and Business Media B.V., pp:1-202.

[2] Y. Yoshihara, T. Igarashi, M. Takeuchi, M. Kawashima, H. Yamaguchi, "A 65-nm SoC Embedded 6T-SRAM Designed for Manufacturability With Read and Write Operation Stabilizing Circuits" IEEE J. Solid-State Circuits, vol. 42, issue 4, pp. 820-829 , April 2007 .

[3] A. P. Chandrakasan el al., "Low-power CMOS digital design," IEEE Journal of Solid-state Circuits", Vol. 27, pp. 473-484, Apr. 1992.

[4] H. Pilo et al., "An 833MHz 1.5W 18Mb CMOS SRAM with 1.67 Gb/s/pin," Proc. IEEEISSCC, pp. 266-267, 2000. T. Uetake et al., "A 1.0 ns access 770MHz 36Kb SRAM Macro," Dig. Symp. VLSI Circuits,pp. 109-110, 1999.

[5] Sleepy Stack: "A New Approach to Low Power VLSI Logic and Memory", Jun Cheol Park.

[6] Jiajing Wang, Satyanand Nalam, and Benton H. Calhoun, "Analyzing Static and Dynamic Write Margin for Nanometer SRAMs", Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA 22904, USA {jw4pg, svn2u,calhoun}@virginia.edu.

[7] Janm Rabaey , Anantha Chandakasan , Borivoje Nikolic ." Digital Integrated Circuits".second edition.

[8] Zheng Guo, Andrew Carlson, Liang-Teck Pang, Kenneth Duong, Tsu-Jae King Liu, Borivoje Nikolic., "Large-Scale Read/Write Margin Measurement in 45nm CMOS SRAM Arrays", Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA.

[9] Arash Azizi Mazreah, Mohammad T. Manzuri Shalmani, Hamid Barati, Ali Barati, and Ali Sarchami., "A Low Power SRAM Base on Novel Word-Line Decoding", World Academy of Science, Engineering and Technology 39 2008.

[10] Saibal Mukhopadhyay, Hamid Mahmoodi, and Kaushik Roy., "Statistical Design and Optimization of SRAM Cell for Yield Enhancement", Dept. of Electrical and Computer Engineering, Purdue University, West Lafayette, IN-47907, USA.

[11] Mamatha Samson, "Performance Analysis of Dual Vt Asymmetric SRAM -Effect of Process Induced Vt Variations", Center for VLSI and Embedded System Technologies Department, International Institute of Information and Technology, Hyderabad, India.

[12] Arash Azizi Mazreah, Mohammad T. Manzuri Shalmani, Hamid Barati, and Ali Barati., "A Novel Four-Transistor SRAM Cell with Low Dynamic Power Consumption", World Academy of Science, Engineering and Technology 39, 2008

[13] Kiyoo Itoh, "VLSI Memory Chip Design," Springer-Verlag Berlin Heidelberg New York, p.p. 110, 2001.

[14] B. S. Amrutur and M. A. Horowitz, "A replica technique for wordline and sense control in low-power SRAM's," IEEE Journal of Solid-state Circuits, Vol. 33, No. 8, pp. 1208- 1218, August 1998.

[15] Tegze P. Haraszti, Microcirc Associates "CMOS Memory Circuits", kluwer academic publishers New York, boston , dordrecht, London, Moscow. Pages 238-239.

[16] Sung-Mo Kang, Yusuf Leblebici,, "CMOS DIGITAL INTEGRATED CIRCUITS", Analysis and Design, McGraw-Hill International Editions, Boston, 2nd Edition, 1999.