Modeling and designing of Sense Amplifier based Flip-Flop using Cadence tool at 45nm

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ABSTRACT- Today to compete the race of improvements and advancements of technological mysteries are lasting upon innovative ideas and noble thoughts. The consequences of using normal Master-Slave Flip-flops in ultra high speed circuits are increase in cycle time, blurredness in clock edge / skew, higher crosstalk / substrate coupling/power consumption/ expensive packaging including cooling systems and limiting performance. An innovative idea of Sense amplifier based Flip-flops (SAFF) has been implemented which can be speed-up the processes up to optimum rate (i.e. Shannon Rate) with compensated SNR. To save the Time Element, designed prototype model to be operated, with ultra high speed for error detection and performance evaluation. Referred to authors previous paper, Modeling and design optimization of Latch Circuits using Parametric Timing Analysis, the latch circuits were thoroughly analyzed w.r.t. their operating speed and its effect over various parameters was discussed, in tighter timing constraints needs to concentrate on power dissipation and durability of device. Overlooking of setup and hold times spans, pays a heavy cost of compromise in the circuits with various latch-ups inducted during design, testing and quality check phase. In sense amplifier- flip-flop (SAFF) based structures, delay can be fairly minimized between the latest point of data arrival and output transition using hybrid latch - flip-flop (HLFF) and semi-dynamic flip-flop (SDFF). SAFF based latch models, consists of the sense amplifier in the first stage and the RS latch in the second stage which are being implemented and simulated by using the Cadence Spectre design tool using 45nm technology. It senses the true and complementary differential inputs and produces monotonous transitions from high to low logic or vice-versa outputs for S-R Latch following the leading clock edge. The S-R latch captures each transition and holds the state until the next leading clock edge arrives, due to this feature; the whole structure becomes a self sustaining flip-flop device.

Keywords
Time Element, parametric timing analysis, setup and hold times, crosstalk, Shannon Rate, Sense amplifier- flip-flop (SAFF).

I. INTRODUCTION

The sense amplifier-based flip-flop may typically include a master latch and a slave latch. A current sensing type sense amplifier (basically a Differential Amplifier) circuit may be used as the master latch, and a setup time of that master latch may be relatively short. A NAND gate type RS latch may be used as the slave latch, in which a relatively stable operation may be maintained at higher clock pulse train accurately. This paper represents a newly developed SAFF that overcomes the major short coming of the previously reported SAFF. In Section II, we present the analysis of the SAFF operation and discuss the drawbacks of the structure that has been commonly used [1]-[4]. Section III reviews the operation of the sense amplifier (SA) as a pulse-generating stage [3, 7]. The section IV presents the design of the slave latch in the second stage. Design Implementation of the new flip-flop, measurement setup using Cadence Virtuoso tools presented in Section V [1, 8, 9, 11]. Section VI presents the summery of SAFF parameters and section VII presents comparison

with recently reported flip-flops, which is followed by a brief conclusion in Section VIII.

II. SENSE-AMPLIFIER-BASED FLIP-FLOP

Let start from, MS (master–slave) latch pair, which is also essential to distinguish as it consisting of two cascaded latches and potentially can be transparent without sufficient margin between the two clocking phases. Generally, flip-flops consist two blocks: a pulse generator (PG) and a slave latch (SL) as shown in fig.1 [1,3,4].

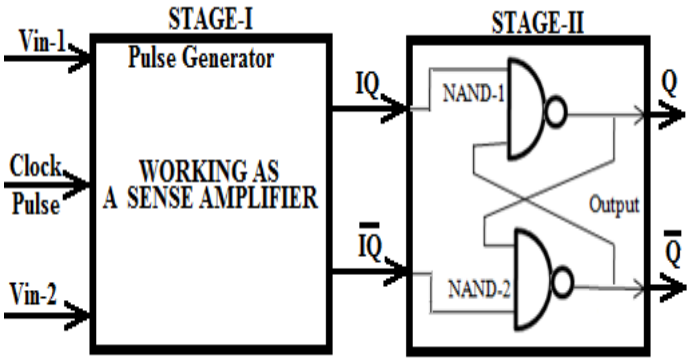

Figure 1. (conventional sense amplifier based design)

The Pulse Generator stage (PG) is a function of the clock and data signals in which a sufficient duration pulse train of clock and data values is produced to Set /Reset the slave latch. Depending on a particular realization, the PG stage is sensitive to the transition of the clock (from low-to-high, or vice- versa) and not to its level, as is not in the case with Master-Slave combination. This sensitivity in the implementation of the PG stage may pose a danger under certain conditions in terms of reliability and robustness while handling complex operations. The SAFF consists of the SA (Sense Amplifier) in the first stage and the slave latch (SR latch) in the second stage as shown in Fig. 2, [7]. Thus SAFF is a flip-flop where the SA stage provides a negative pulse on one of the inputs to the slave latch or depending whether the output is to be set or reset. It senses the true and complementary differential inputs. The SA stage produces monotonic transitions from one to zero logic level on one of the outputs, following the leading clock edge.

III. REVIEW OF THE PULSE-GENERATING STAGE OPERATION

When low, nodes are labeled and pre-charged through small NMOS and PMOS transistors, as in Fig. 2. The lower limit on the size of these transistors is determined by their capability to pre-charge the nodes in one half of the cycle. The high state off and on keeps charging their sources up to critical value because there is no path to ground due to the off state of the clocked transistor. Since either or is on and the common node is also pre-charged, Therefore, prior to the leading clock edge, all the capacitances in the differential tree are pre-charged.

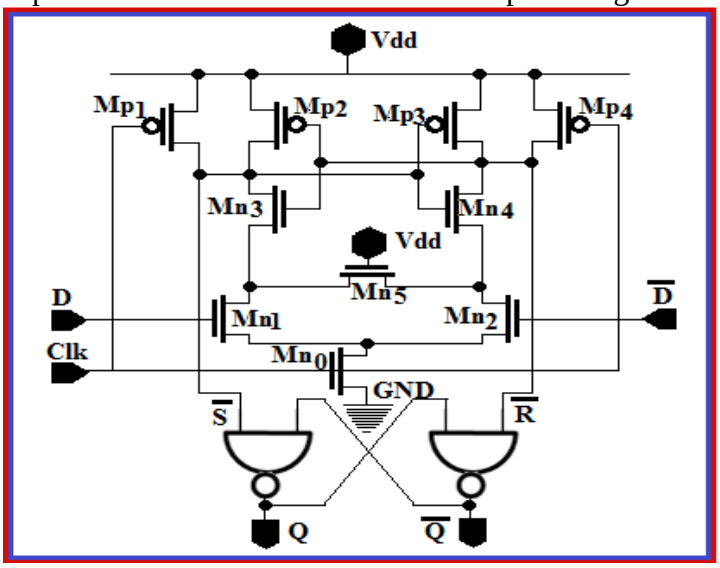

Figure 2.(Pulse Generating stage of differential amplifier)

IV. SYMMETRIC SLAVE LATCH

The SR latch of the SAFF, shown in Fig. 3, operates as follows: input **S** is a set input and **R** is a reset input. The simultaneous low or high voltage level at both and node is not permitted which is guaranteed by the SA stage. Therefore, one of the output signals will always be delayed with respect to the other. The rising edge always occurs first, after one gate delay, and the falling edge occurs after two gate delays, additionally the delay of the true output depends on the load on the complementary output, this limits the performance of the SAFF[10,15]. In order to overcome the problem of non-symmetry of the SR latch in SAFF, modifications to be applied in the SL stage. The following description, represents a future state of the SL, i.e., the state after the transition of the clock. The SL modification starts with logic representations for the new output values and that are obtained by writing independent logic equations and outputs of the cross-coupled NAND gate SR latch. Initial stage is implemented as an

AND-OR structure, where is an OR branch of the circuit used to implement this expression.

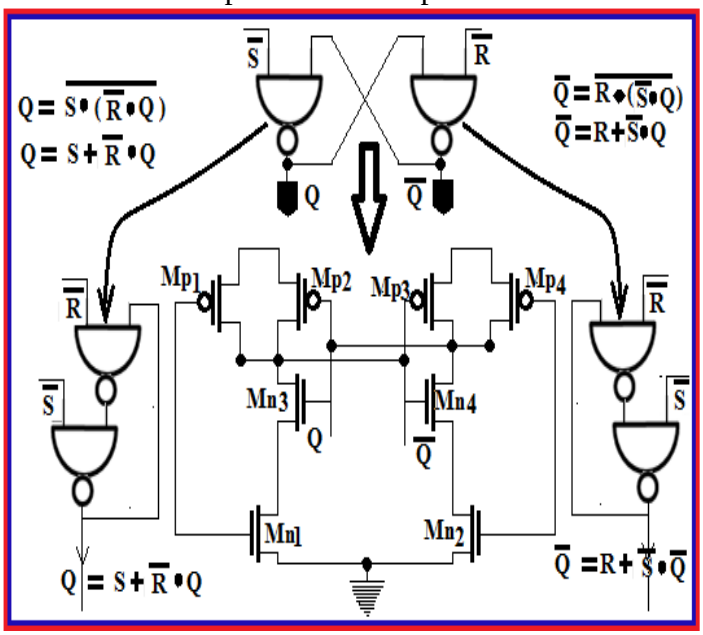

Figure 3.(Triggering of Symmetric Slave latch)

The SA stage is triggered on the leading edge of the clock. If is high, node is discharged through the path turning off and on. After this initial change, further changes of data inputs will not affect the state of the AND nodes. The inputs are decoupled from the outputs of the SA, forming the base for the flip-flop operation in the circuit. The output of the SA, which is forced to low at the leading edge of the clock, becomes floating low if the data changes during the high clock pulse. The additional transistor allows static operation, providing a path to ground even after the data is changed. This prevents the potential charging of the low output of the SA stage, due to the leakage currents. However, the additional transistor forces the whole differential tree to be pre-charged and discharged in every clock cycle, independent of the state of the data after the leading edge of the clock. The additional transistor is minimized, to prevent a significant increase in delay of the SA stage, due to the simultaneous discharging of both the direct path capacitive load and the load of the opposite branch. This flip-flop has differential inputs and is suitable for use with differential and reduced swing logic. It uses single-phase clock, and has small clock load. Its first stage assures accurate timing, due to its SA topology, which plays a very important role at high operating frequencies. After this initial change, further changes of data inputs will not affect the state of the and nodes. The inputs are decoupled from the outputs of the SA forming the base for the flip-flop operation of the circuit. The output of the SA, which is forced to low at the leading edge of the clock, becomes floating low if the data changes during the high clock pulse. The additional transistor allows static operation, providing a path to ground even after the data is changed. This prevents the potential charging of the low output of the SA stage, due to the leakage currents. However, the additional transistor forces the whole differential tree to be pre-charged and discharged in every clock cycle, independent of the state of the data after the leading edge of the clock. The additional transistor is minimized, to prevent a significant increase in delay of the SA stage, due to the simultaneous discharging of both the direct path capacitive load and the load of the opposite branch. This flip-flop has differential inputs and is suitable for use with differential and reduced swing logic. It uses single-phase clock, and has small clock load. Its first stage assures accurate timing, due to its SA topology, which plays a a very important role at high operating frequencies. The SA stage is triggered on the leading edge of the clock. If is high, node is discharged through the path turning off and on. After this initial change, further changes of data inputs will not affect the state of the and nodes. The inputs are decoupled from the outputs of the SA forming the base for the flip-flop operation of the circuit. The output of the SA, which is forced to low at the leading edge of the clock, becomes floating low if the data changes during the high clock pulse. The additional transistor allows static operation, providing a path to ground even after the data is changed. This prevents the potential charging of the low output of the SA stage, due to the leakage currents. However, the additional transistor forces the whole differential tree to be pre-charged and discharged in every clock cycle, independent of the state of the data after the leading edge of the clock. The additional transistor is minimized, to prevent a significant increase in delay of the SA stage, due to the simultaneous discharging of both the direct path capacitive load and the load of the opposite branch. This flip-flop has differential inputs and is suitable for use with differential and reduced swing logic. It uses single-phase clock, and has small clock load. Its first stage assures accurate timing, due to its SA topology, which plays a a very important role at high operating frequencies.

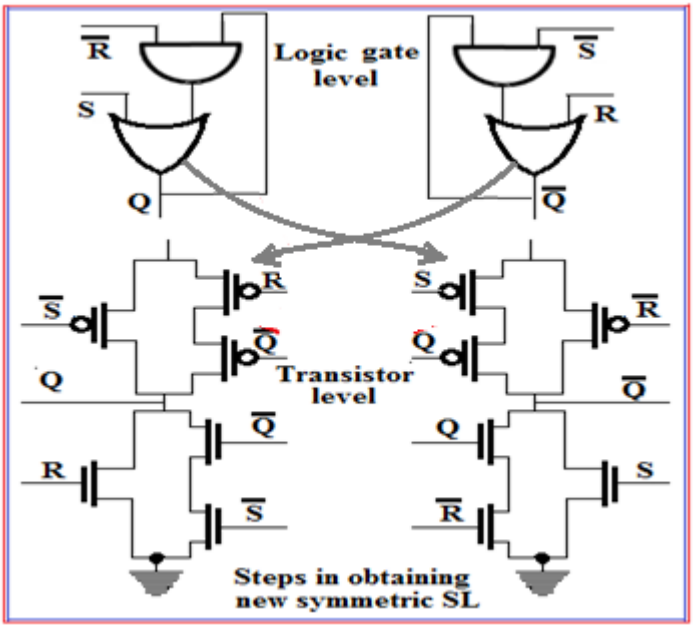

Figure 4. (New symmetric of SAFF)

In order to drive the load and to change the state of the latch, as illustrated in Fig. 4. This feature makes output transistor size optimization, minimization, robustness, crosstalk, crow-bar current, reduction in power dissipation. Reduced clock-swing operation [10]. The single-ended input version with multiplexed data scan and asynchronous reset is possible as shown in Fig. 5.

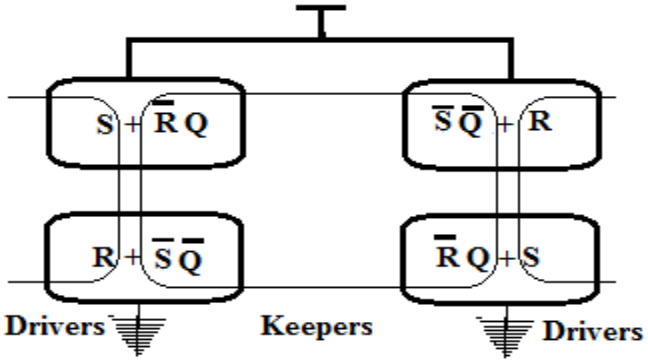

Figure 5. (Modified SAFF)

V. DESIGN IMPLEMENTATION AND MEASUREMENTS

The proposed schematic as shown in Fig. 6 has been designed using Cadence 45 nm scale technology and implemented various test like DRC (design rule check,), ASSURA LVS and design extracted with RCX. The new SAFF is designed and implemented in 45 nm effective channel length CMOS technology.

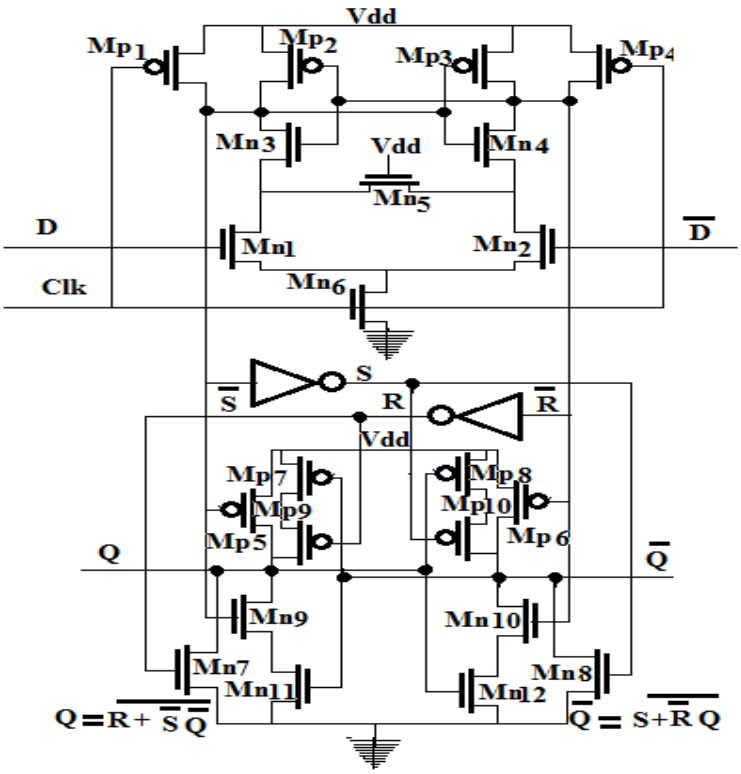

Figure 6. (Proposed transistor level circuit diagram)

Transistor sizing is optimized using iterative procedure with the objective of achieving high speed and compact grid-based layout. In order to measure the flip-flop performance, a simple test structure was designed and implemented using 45 nm Cadence Virtuoso tool as shown in Fig.7.

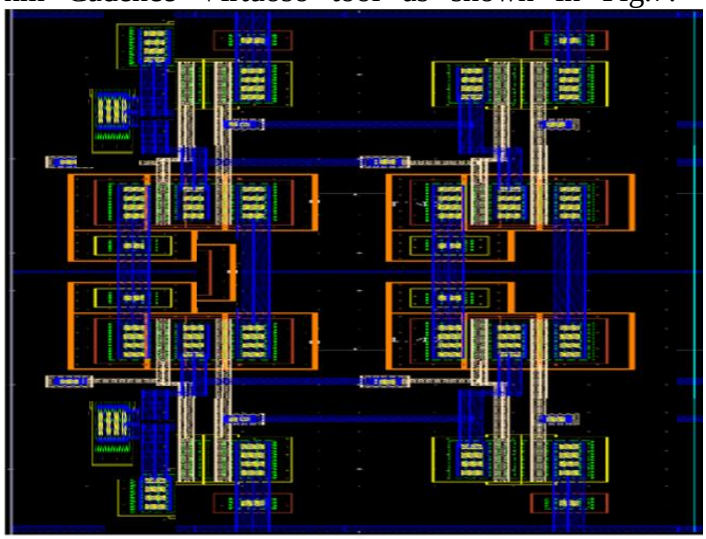

Figure 7. (Layout: Proposed SAFF)

Illustrating from input data the minimum delay between the latest point of data arrival and output transition is measured indirectly, using the structure from Fig. 08.

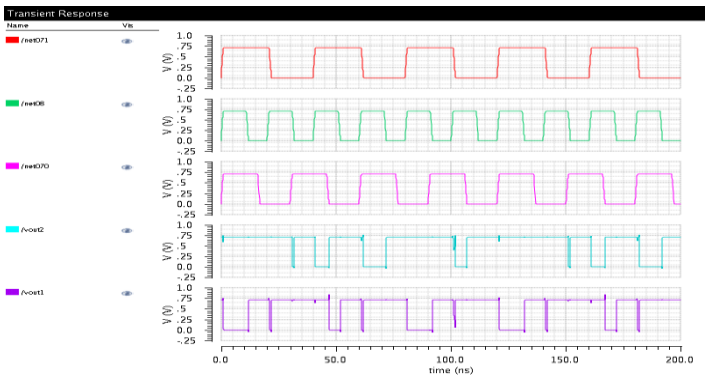

Figure 8. (Timing Diagram)

As depicted from Fig. 9. several chains of inverters as depicted in Fig. 7, were implemented. The test chip contained a time-base generator, which allowed wide variation of clock time period with resolution of 15 ns to 1.25 ns. The clock frequency was raised until one of the flip-flops receiving signal from a chain of inverters failed.

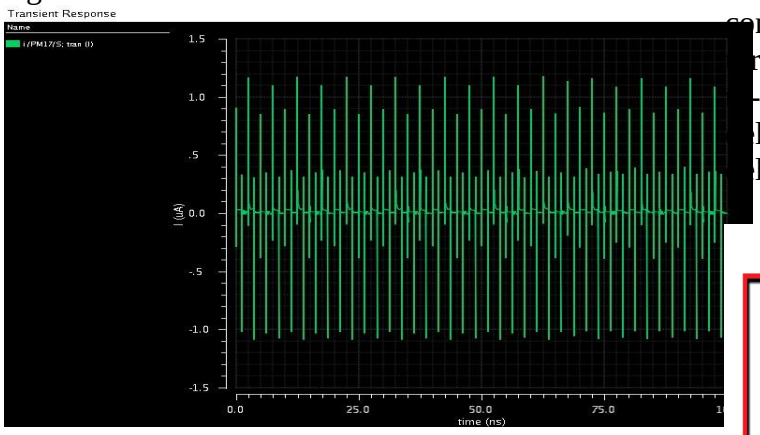

Figure 9. (Average Leakage current)

The time period corresponding to the failing clock frequency was calculated and entered into a set of equations describing the timing relationship between the flip-flop parameters and the signal delay as depicted in Fig. 10.

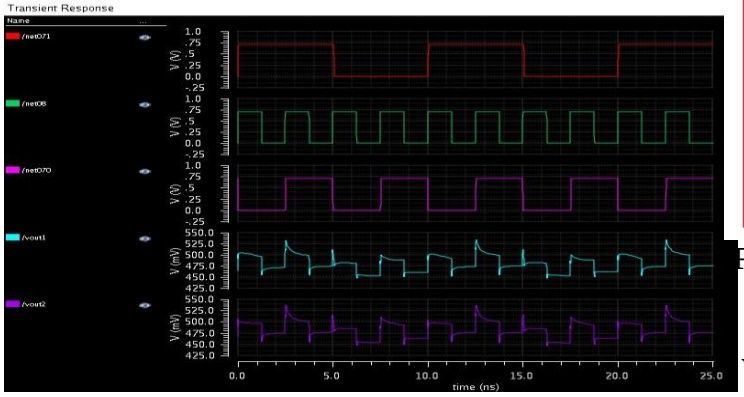

Figure 10. (Timing Diagram of failing clock frequency)

The clock frequency was changed in the 50–700 MHz range using an on-chip time-base generator. The clock frequency was gradually increased until each off our paths fail to satisfy the setup timings and results as reflected by Fig. 11.

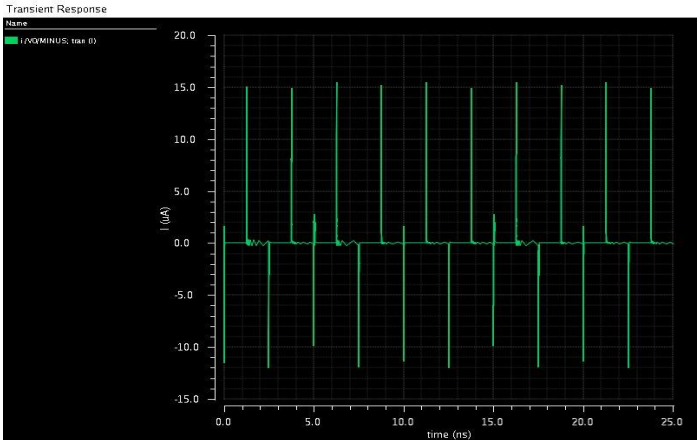

Figure 11. (Average Leakage Current of failing setup timings)

The inverter chain used in this measurement consisted of up to eight cells. Each cell consisted of three inverters with balanced high-to-low and low-to-high delays. Whereas Fig. 12 represents a cell delay with fan-out of one inverter and is the cell delay with fan-out of two.

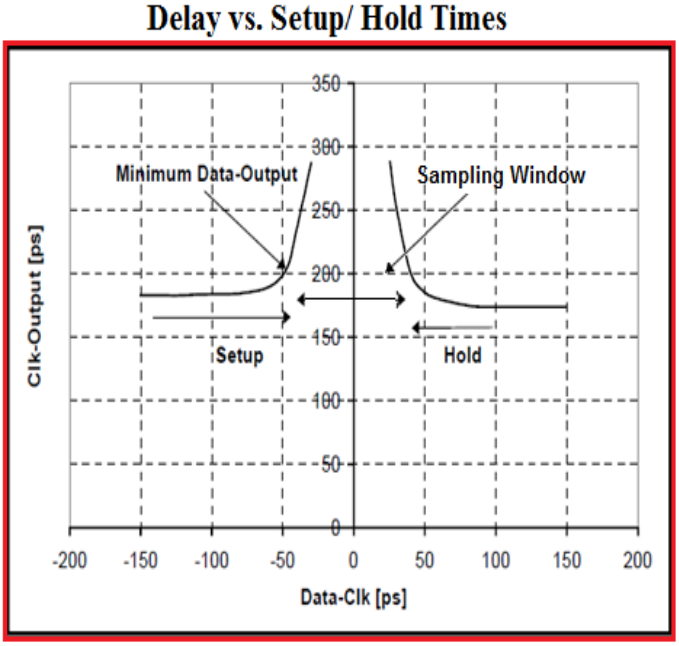

Figure 11. (Average Cell delay in setup timings)

VI. SUMMARY OF SAFF PARAMETERS OF SCHEMATIC LAYOUT

All the observations and test results are evaluated from schematic layout diagram using Cadence

Virtuoso Tool at 45 nm scale at Vdd=0.7V and $T=300^0$ K.

Parameters	Test result #01 Clk pulse 15 ns	Test result #02 Clk pulse 10 ns	Test result #03 Clk pulse 05 ns	Test result #04 Clk pulse 2.5 ns	Test result #05 Clk pulse 1.25 ns
Rise time Delay	102 P-Sec	105 P-Sec	112 P-Sec	117 P-Sec	126 P-Sec
Fall Time Delay	110 P-Sec	129 P-Sec	142 P-Sec	160 P-Sec	161 P-Sec
Setup Time	200 P-Sec	211.5 P-Sec	220.5 P-Sec	220.7 P-Sec	221.6 P-Sec
Hold Time	67 P-Sec	80.9 P-Sec	84 P-Sec	85.9 P-Sec	91 P-Sec
Average Total Current	-35.96 n-Amp	61.38 n-Amp	87.99 n-Amp	101.50 n-Amp	251.4 n-Amp
Average Leakage Current	13.56 n-Amp	14.91 n-Amp	15.64 n-Amp	19.63 n-Amp	20.40 n-Amp
Average Power	40.43 n-Watt	45.09 n-Watt	90.66 n-Watt	126.99n-Watt	131.3 n-Watt
Average Leakage Power	13.34 n-Watt	15.54 n-Watt	17.91 n-Watt	19.59 n-Watt	22.52 n-Watt

VII. COMPARISON WITH RELATED FLIP-FLOPS

The interest in high-speed flip-flop design re-emerged recently as the frequencies of operation passed 1 GHz. The importance of a good flip-flop design affects the power consumed by the clock as well as the available time in ever-shrinking pipeline. Many new latch and flip-flop architectures were published [4], [7]–[9], [12]–[21]. They demonstrated improvements in speed, power, reliability, clock load, setup and hold times. Flip-flop performance comparison with respect to speed and power dissipation in this work is done resembling the setup in [3], [11]. In comparison to other recently published flip-flops, HLFF modified SA flip-flop has the shortest delay, represented by the sum of setup time and clock to output delay[15-16]. Power consumption in Fig. 15 is shown for maximum, average, and minimum activities of the data input. Table II shows the total gate length of all compared flip-flops, as an area estimate. The improved SAFF is about 20% larger than SDFF and HLFF, with a 5%–10% increase in speed, but features differential outputs, that both can drive the loads. The SAFF size can be reduced by about 5%, with small increase in speed if only one output is used.

VIII. CONCLUSION

We developed, fabricated and tested an improved SA flip-flop using Cadence Spectre design tool in 45nm technology. We presented a systematic method for its derivation, which allows flip-flop realization in a circuit topology yielding operational needs. This paper introduces new sense amplifier based flip-flop. The slave latch of the new flip-flop is able to keep the advantage of NC2MOS approach [15]. The design can be used as an energy recovery flip-flop, since it is assumed that only the storage part of element of flip flop cannot be energy recovering because they drive standard (non-adiabatic) logic [9]. But the energy at the gates of sense amplifiers can be used for energy recovery, since they are not the part of storage element. However, the proposed design is more efficient due to feed back inverters used and consumes lesser total power when compared with conventional and Hybrid flip-flops. The proposed flip-flop gives a very good PDP with glitch free operation, lesser crow-bar current and lesser static power Increase. A new design of sense-amplifier-based flip-flop is presented that eliminates floating nodes in the sensed train of pulses and outperforms earlier presented latch design implementation used in high-performance processors.

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