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# Analysis of Junction less Transistor

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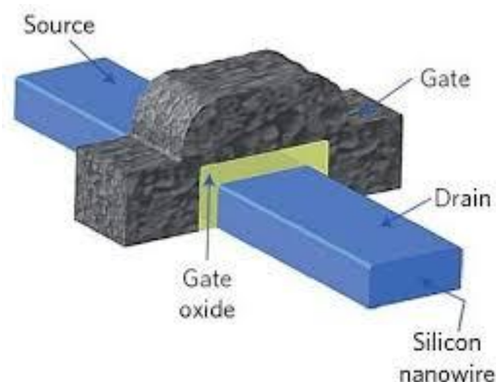
***Abstract-* We present the fabrication, electrical characteristics, and effect of lateral gates in a junction less silicon nano wire transistor The transistor uses silicon nanowire on silicon-on-insulator wafer fabricated with an atomic force microscope nanolithography technique. Using AFM nanolithography allows us to make a chemical contrast between locally oxidized part of the surface and unexposed surface. This chemical contrast affects as a mask and the active part of the device is finally obtained after two step etching. The structure is uniformly low-doped for source, drain, channel, and the lateral gates regions, and confirms the behavior of junctionless nanowire transistors. The output current is controlled by channel doping and mobility of carriers instead of gate capacitance and it basically uses bulk conduction instead of surface channel conduction. The fabricated device exhibits an on-off ratio of 2×106 and a subthreshold swing of 160 mV/decade.**

## OBJECTIVE OF JUNCTIONLESS TANSISTOR

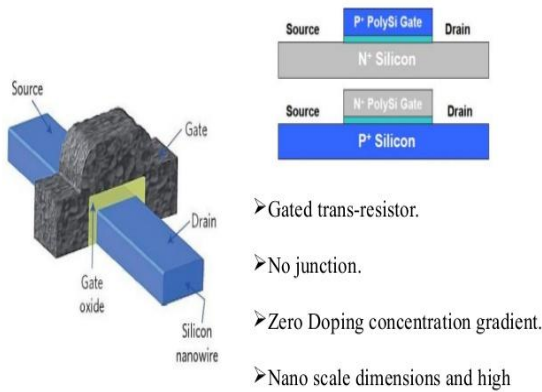
**Junctionless nanowire transistor** (JNT) also say junction less transistor is a nanowire-based transistor that has no gate junction because Junctions are difficult to fabricate, and, because they are a significant source of current leakage, they waste significant power and heat. Junctionless transistors are variable resistors controlled by a gate electrode. The silicon channel is a heavily doped nanowire that can be fully depleted to turn the device off. The electrical characteristics are identical to those of normal MOS-FETs, but the physics is quite different. Conduction mechanisms in Junctionless Nanowire Transistors (gated resistors) are compared to inversion-mode and accumulation-mode MOS devices. The junctionless device uses bulk conduction instead of surface channel conduction. The current drive is controlled by doping concentration and not by gate capacitance. The variation of threshold voltage with physical parameters and intrinsic device performance is analyzed. A scheme is proposed for the fabrication of the devices on bulk silicon.This method has been described as akin to squeezing a garden hose to gate the flow of water through the hose. The nanowire is heavily n-doped, making it an excellent conductor. Crucially the gate, comprising silicon, is heavily p-doped; and its presence depletes the underlying silicon nanowire thereby preventing carrier flow past the gate.

Thus the device is turned off not by reverse bias voltage applied to the gate, as in the case of conventional MOSFET but by full depletion of the channel. This depletion is caused due to work-function difference (Contact_potentials) between the gate material and doped silicon in the nanowire.

This combination of n-doped nanowire and the p-doped channel forms a p–n junction and depletion layer is formed. Due to heavy concentration of the dopant atom in both nanowire and gate the depletion region is so large that virtually no carriers are present to conduct the current. When a forward bias voltage is applied the thickness of the depletion region is reduced and gradually the channel forms which causes the current to flow again.The JNT uses bulk conduction instead of surface channel conduction. The current drive is controlled by doping concentration and not by gate capacitance



## STRUCTURE OF JUNCTIONLESS TRANSISTOR




## ADVANTAGES

The electric field perpendicular to the current flow is found to be significantly lower in junctionless transistors than in regular inversion-mode or accumulation-mode field-effect transistors. Since inversion channel mobility in metal-oxide-semionductor transistors is reduced by this electric field, the low field in junctionless transistor may give them an advantage in terms of current drive for nanometer-scale complementary metal-oxide semiconductor applications. This observation still applies when quantum confinement is present. The electric field perpendicular to the current flow is found to be significantly lower in junctionless transistors than in regular inversion-mode or accumulation-mode field-effect transistors. Since inversion channel mobility in metal-oxide-semionductor transistors is reduced by this electric field, the low field in junctionless transistor may give them an advantage in terms of current drive for nanometer-scale complementary metal-oxide semiconductor applications. This observation still applies when quantum confinement is present.

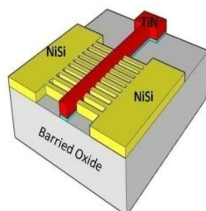



Fig.1 Depicts schematically view of the high-K metal-gate nanowire junctionlessFinFET.

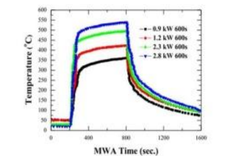



Fig2 Comparisons of temperature profiles versus MWA time at different MWA power.

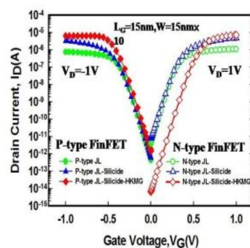
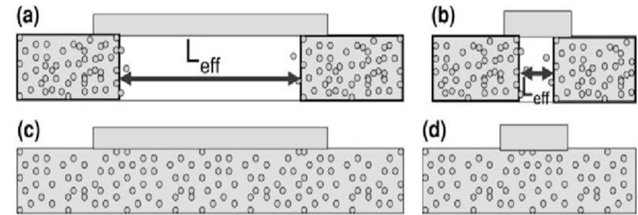



Fig.3 $I_D$–$V_G$ characteristics of a 15 nm gate-length high-k metal-gate nanowire junctionlessFinFET

## DISADVANTAGES

1. Decreases mobility.
2. Conventional junctionless transistor is that they suffer from poor short channel effect.




Scattering of source and drain doping impurities in the channel of a a long-channel and b a short-channel inversion-mode MOSFETs; c long-channel and d short-channel junctionless devices.

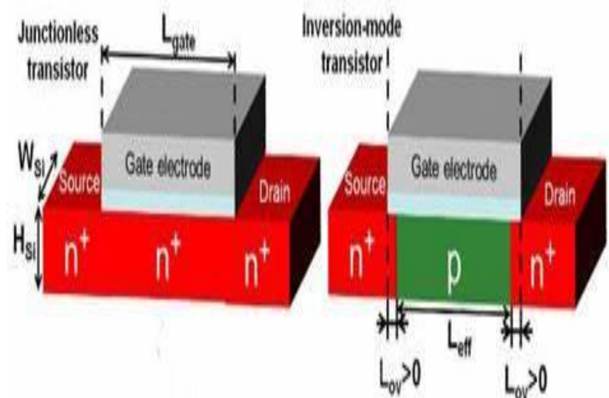
## METHODOLOGY

We All Know Transistor Are The All Building Blocks of all modern elctric devices.
All existing transistor have junctiion.
Bjt- two p-n junctioins .
Mesfet- schotty junction.

So, There is some disadvantages of junctions:
1. Decrease mobility.
2. Heat dissipitaion.
3. Difficult and expensive to fabricate.
4. Source of current leakeage.

## REVOLUTION OF JUNCTIONLESS TRANSISTOR

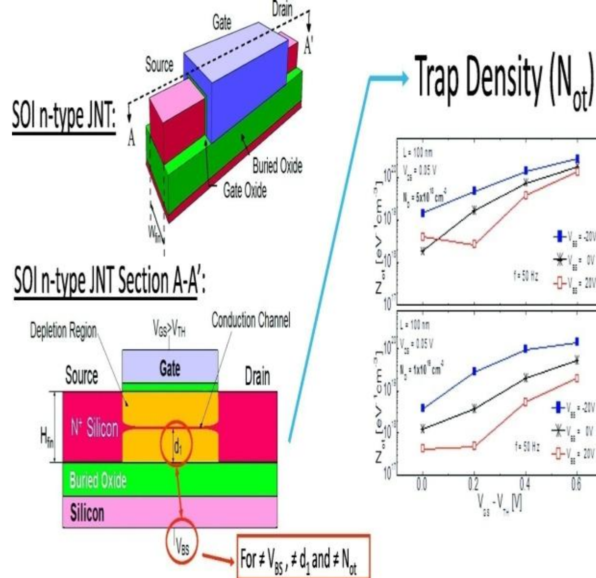
Junctioinless transistor was invented by Tyndall National institute, Ireland in 2010.




The device basically a resistor in which the mobile carrier can be modulated by Gate.

Uniform doped nano wire without junction with a wrap – around gate.

This work reports on the integration of n-type lateral-drain-extended MOS transistors (LDMOS) in a 0.13 µm SiGe BiCMOS technology. The transistors are realized with no additional process steps using the core dual-gate-oxide CMOS flow only. LDMOS drift regions are formed by compensating lightly-doped drain (LDD) implantations of NMOS and PMOS transistors of the baseline process. Stable operation with less than 10% parameter variations in 10 years is achieved up to operating voltages VDD,max of 10 V for devices with breakdown voltages BVDSS = 30 V and on-resistances RON = 7.3 Ω mm. Devices for different operating voltages VDD,max are realized by layout variations. Devices with VDD,max = 6 V demonstrate breakdown voltages BVDSS = 25 V, on-resistances RON = 4.9 Ω mm, and peak transit frequencies fT = 32 GHz.

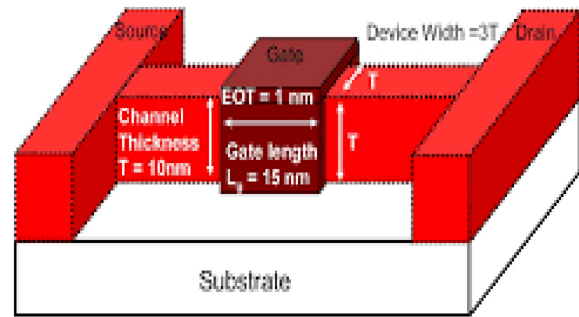



## FABRICATION PROCESS

Doping concentration is constant and uniform throught the device and typically

Ranges from 10^19 and 10^20cm.

The device features bulk conduction instead of source conduction.




| Device Structure | JL Bulk FinFET | SOI JNT |
|---|---|---|
| Gate Workfunction | N: 4.76 eV<br>P: 4.52 eV | N: 5.0 eV<br>P: 4.3 eV |
| Source/Drain/Channel Doping Concentration | N: $1.5x10^{19}cm^{-3}$<br>P: $1.5x10^{19}cm^{-3}$ | N: $1.5x10^{19}cm^{-3}$<br>P: $1.5x10^{19}cm^{-3}$ |
| Substrate Material | Silicon with<br>N: $5x10^{18}cm^{-3}$, P-type<br>P: $5x10^{18}cm^{-3}$, N-type | $SiO_2$ |

Uniform Doping concentration .

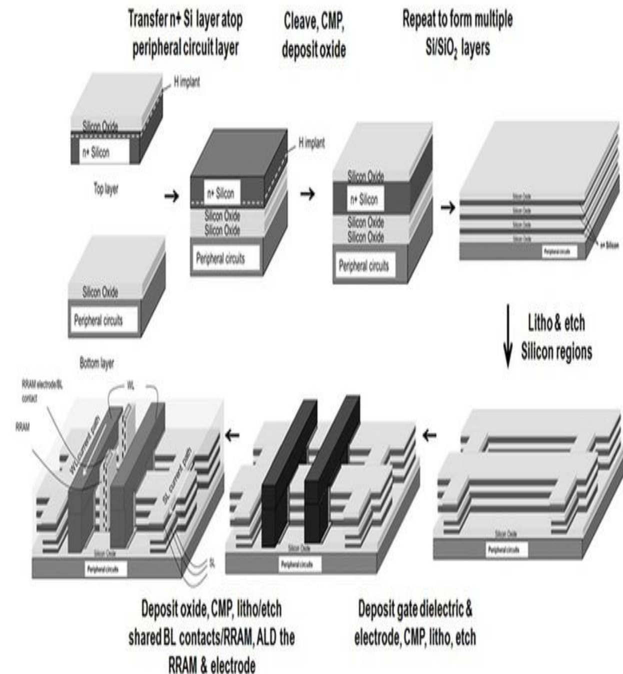
Bulk conduction.

Beam lithrography for nonowire and gates.

For n-channel dopant ARESNIC Channel concentration :

Gate material : P+ POLYSILLICON.

Temperature dependence.

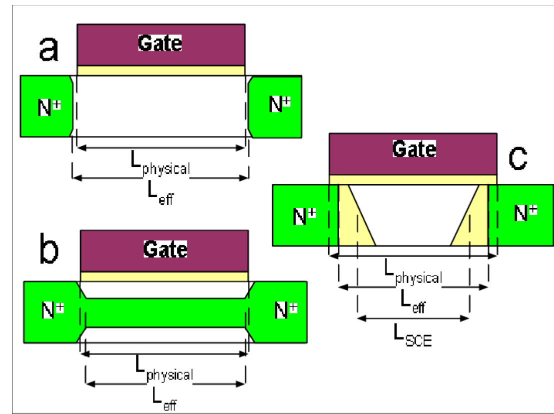


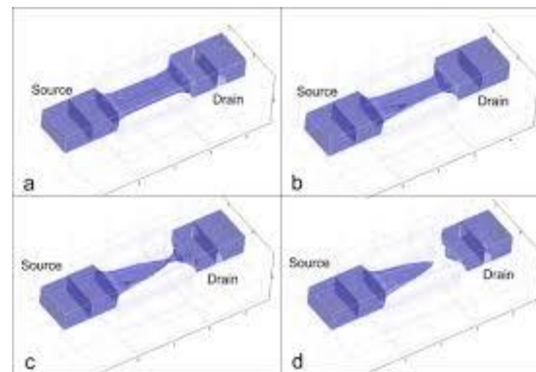

Semiconductor is doped so heaviely that it allow reasonable current flow when on.

This combination of n-doped nanowire and the p-doped channel forms a p–n junction and depletion layer is formed. Due to heavy concentration of the dopant atom in both nanowire and gate the depletion region is so large that virtually no carriers are present to conduct the current. When a forward bias voltage is applied the thickness of the depletion region is reduced and gradually the channel forms which causes the current to flow againThe device is fabricated by atomic force microscopy nanolithography on silicon-on-insulator wafer. The output and transfer characteristics of the device are obtained using 3-D Technology Computer Aided Design (TCAD) Sentaurus software and compared with experimental measurement results. The advantages of AFM nanolithography in contact mode and Silicon on Insulator (SOI) technology were implemented to fabricate a simple structure which exhibits the behaviour of field effect transistors. The device has 200-nm channel length, 100-nm gate gap and 4 μm for the distance between the source and drain contacts. The characteristics of the fabricated device were measured using an Agilent HP4156C semiconductor parameter analyzer (SPA). A 3-D TCAD Sentaurus tool is used as the simulation platform. The Boltzmann statistics is adopted because of the low doping concentration of the channel. Hydrodynamic model is taken to be as the main transport model for all simulations, and the quantum mechanical effects are ignored. A doping dependent Masetti mobility model was also included as well as an electric field dependent model with Shockley–Read–Hall (SRH) carrier recombination/generation.

## WORKING OF JUNCTIONLESS TRANSISTOR

This work presents, for the first time, an experimental analysis of the low-frequency noise and the effective trap density dependence of junctionless nanowire transistors (JNTs) on the substrate bias. The study has been performed for devices with different channel lengths and doping concentrations biased close to the threshold and deep in linear regime. It has been shown that the surface potential of JNTs is strongly influenced by the substrate bias even above threshold. Thus, the drain current noise spectral density and the effective trap density can be improved or degraded depending on the bias applied to the substrate of the devices. Additionally, it is shown that, the variation on the substrate bias enables the evaluation of traps with different activation energy ranges, which is more evident in heavier doped devices due to the higher threshold voltage sensitivity to the substrate bias




Increase GATE voltage at vd of 50 mv.
Increase DRAIN voltage.
Measured ID(VD) OF N-AND P-channel junctionless transistors L=1um,W=20nm.
Measured ID (VG) of N-channel junctionless transistor L=1um,W=20nm versus gate voltage,VG for a drain voltage of+1 Vin t-type and p-type device having a width of 30nm and a length of 1nm.

## SHORT CHANNEL EFFECT

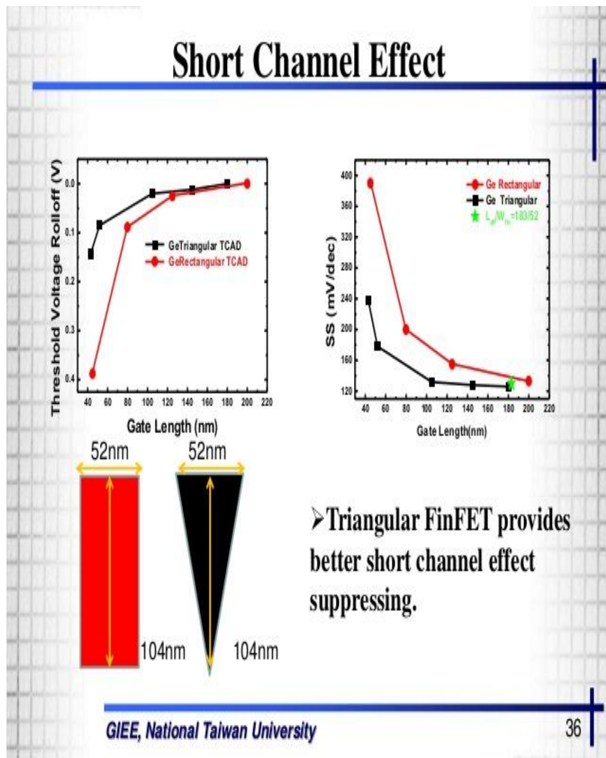
Short channel effect is an effect in which the channel length is same order of magnitude as the depletion layer width of the source and the drain.

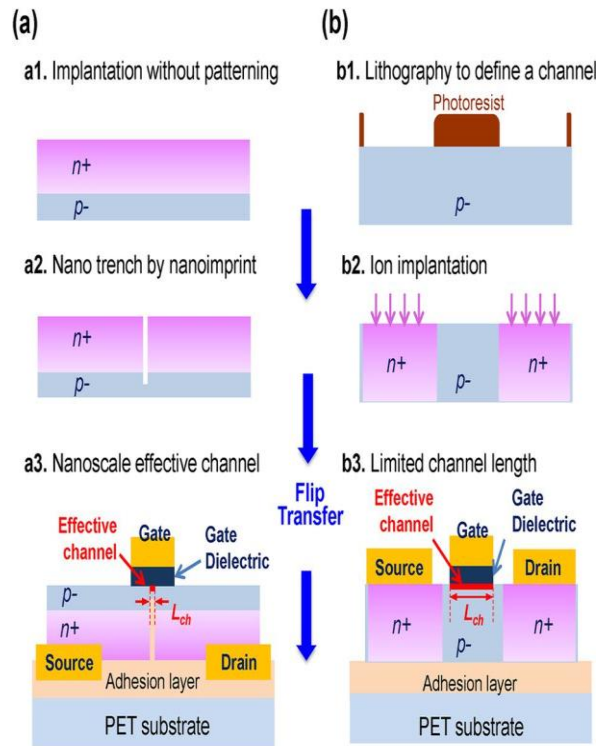
Drain induced barrier lowering(increase in vt with vd) is less important in junctionless transistor.

NO hot electron effect.

Short-channel effects (SCEs) in junctionless (JL) double-gate (DG) MOSFETs analytically by solving the 2-D potential in subthreshold. Ids-Vg curves and Vt rolloff generated from the model are validated by 2-D numerical simulations (Technology Computer Aided Design). It is shown that the SCE of JL MOSFETs is inherently worse

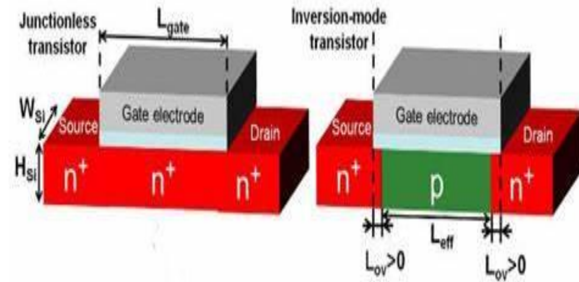
than that of undoped DG MOSFETs. The SCE worsens with increasing doping concentration in the channel.




Properties Of Junction Less Transistor

Basically, drian current increase with doping and channel thickness . Leakage current increase with channel length thickness and doping. Conduction mechanisms in junctionless nanowire transistors (gated resistors) are compared to inversion-mode and accumulation-mode MOS devices. The junctionless device uses bulk conduction instead of surface channel. The current drive is controlled by doping concentration and not by gate capacitance. The variation of threshold voltage with physical parameters and intrinsic device performance is analyzed. A scheme is proposed for the fabrication of the devices on bulk silicon.




Dielectric constant: gate control improves with dielectric constant.

Short channel effect are drastically reduced with scattering properties decreases with increases in gate voltages. It has also threshold variability ,that is, voltage variation is double than conventional devices.

## Types of Junctionless Transistor

### 1. Junctionless nanowire transistor

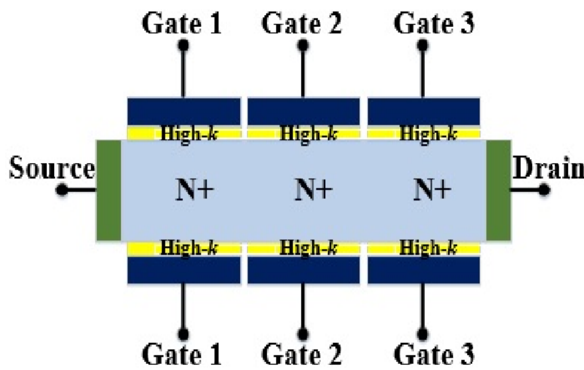
Conduction ,mechanism in junctionless nanowire transistor(gate resistor) are compared to inversion mode and accumulation-mode MOS device.

The junctioless transistor devices use bulk conduction instead of surface channel. The current device controlled by doping concentration and not by gate capacitance. The variation of threshold

Voltage with physical parameter and intrinsic device performance is analyzed.

### 2. Junctionless Tunnel Field effect Transistor:

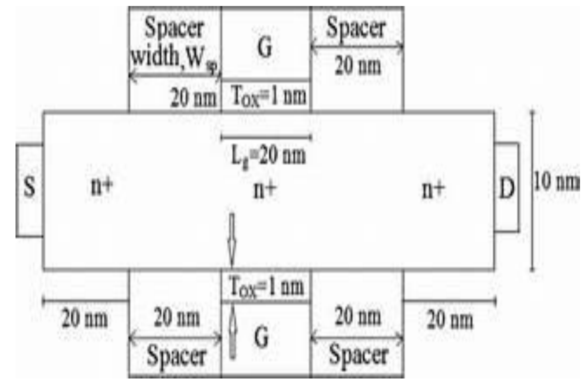
The JL-TFET is a Si-channel heavily doped Junctionless field effect transistor which uses two isolated gates(Control-Gate,P-gate) with two different metal works function to behave like a tunnel filed effect transistor also pereform good switching perfomance,



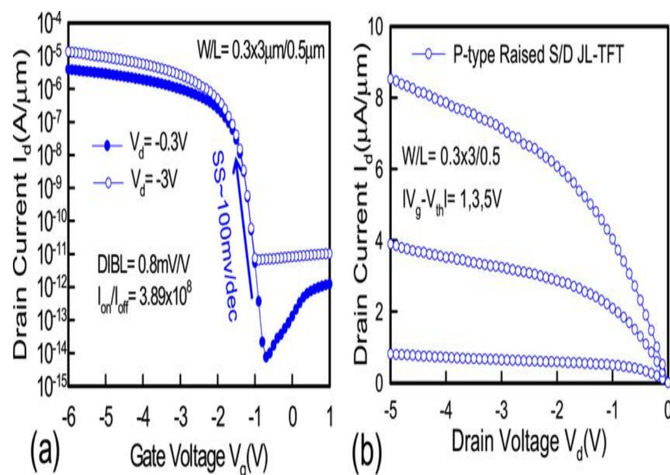

Future Aspect Of Junctionless Transistor

During the recent years, numerous efforts have been made to do real crossing from microelectronics to nanoelectronics and to persist with scaling imposed by Moore's law. Several technological innovations and new materials such as high κ dielectrics, metal gate electrodes, and stressors have been introduced in the fabrication process. Moreover, new transistor architectures based on silicon-on-insulator (SOI), such as FinFETs, multi-gate FETs, omega-gate FETs, and gate-all-around FETs transistors have emerged. Photolithography approaches to the limitation of its potential, in terms of resolution and flexibility. As an alternative among the low cost routes of lithography nano-contact printing technique and atomic force microscopy (AFM) nanolithography are the promising techniques. AFM lithography and scanning tunneling microscopy (STM) lithography are belong to a group of lithography called scanning probe lithography (SPL), which is considered as one of the best lithographic technique for forming nanostructures.

In this paper future of junctionless transistor it give better voltage control and reduced complexity will
Density of transistor per chip. Basically what happen see it the analog properties of nMOS junctionless (JL) multigate transistors, comparing their performance with those exhibited by inversion-mode (IM) trigate devices of similar dimensions. The study has been performed for devices operating in saturation as single-transistor amplifiers, and we have considered the dependence of the analog properties on fin width Wfin and temperature T. Furthermore, this paper aims at providing a physical insight into the analog parameters of JL transistors. For that, in addition to device characterization, 3-D device simulations were performed. It is shown that, depending on gate voltage, JL devices can present both larger Early voltage VEA and larger intrinsic voltage gain AV than IM devices of similar dimensions. In addition, VEA and AV are always improved in JL devices when the temperature is increased, whereas they present a maximum value around room temperature for IM transistors.




We created channel forms between source and drain, in the center of channel, until the peak of the hole concentration in the channel reaches the doping concentration NA. when the device is turned on it approaches the flat band condition, thus, it basically behaves as a resistor and the electric field perpendicular to the current flow is basically equal to zero in the ''bulk'' channel. In fact, as the advantage of the AFM nanolithography the body of the upper Si layer of the SOI, intact and untouched. So we expect to find more bulk property, higher mobility, and less surface scattering effect for the channel under the gate. Moreover, since the system is in ON at VG=0 V, one can say that the threshold voltage is shifted into the positive voltage. That is the reason one can claim the device is like the pinch off transistors and is already in flatband condition. With increasing the positive gate voltage, area under the gates starts to deplete and a sufficient positive bias applied to the gate completely depletes the region. Due to the same doping of structure the channel under the gates cannot invert easily. Even if it were to invert, the reverse bias p-region contacting this inversion layer (-VDS), would limit the transport in this layer. Shows the drain current (ID) versus gate voltage (VG), for a drain voltage of -1 V. The on/off current ratio for gate voltage between 0 and 2 V is around 2×106 for a device with 95 nm width and 100 nm gate gaps. Below threshold voltage of the device, it is possible to apply a sufficient negative gate bias (–VG) to create an accumulation channel and increase the output current (not shown).




In this case the gate acts as a backgate and accumulates the region under the gates. These results are in agreement with the basic theory of junctionless transistors and results obtained and reported by simulation[33] and experimental results in the literature. Shows the simple comparison between the AMOSFET and JLGSNWT holes transmission location path through the channel. It is worth to mention that, due to the device design the accumulation channel will be formed at the bottom of the channel which is the Si/SiO2 interface.

## CONCLUSION ON JUNCTIONLESS TRANSISTOR

We presented here the electrical characteristics of lightly doped junctionless lateral gate silicon nanowire transistors. The fabrication method used is based on AFM nanolithography on SOI substrate. The performance of device is compared to junctionless nanowire transistors. This device is a normally on device which has an off state base on depletion of the channel by electric field originated from the lateral gates. Output current of the device increases strongly with active region doping density and carriers' mobility and it is not depends on the gate capacitance. The device uses bulk conduction instead of surface conduction. Controlling the cross section and gate gaps are key parameters for better performance of the device and particularly for subthreshold swing tuning.

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