Analysis of Performance Metric of FinFET Based SRAM Cell

Meenakshi
Department of Electronics & Communication
Rama University ,Uttar Pradesh, Kanpur, India
Chaudharymeenu001@gmail.com

Abstract –In today's world scenario more than 85-90% of the chip area is mainly occupied by memory.There is a need for faster and reliable memory system for various integrated devices from computers to various handheld devices.In this paper the analysis of SNM, RNM, WNM and static power variation with width of access, load and driver have been carried out for nanoscale FinFET based SRAM cell. FinFET based SRAM design has been proposed as an alternative solution to the bulk devices. It can be inferred from the results that with increase in the width of driver FinFET, the high SNM reduces and low SNM increases.This is due the fact that the leakage current is considerably reduced due to increased control of the FinFET device structure, resulting relatively in high Ion/Ioff ratio. In this work we also analyze the effect of temperature on noise margins and static power for FinFET based SRAM cell. FinFET is suitable for future nanoscale memory circuits design due to its reduced Short Channel Effects (SCE) and leakage current.

Keywords- FinFET, SRAM Cell, SNM, Read Delay

I. INTRODUCTION

The past 4-5 decades CMOS scaling from one technology node to the next node has given improved performance. This enabled in developing smaller, faster and powerful digital systems. But scaling of bulk CMOS is facing a lot of challenges due to material and process technology limits [1]. As per 2011 International Technology Roadmap for Semiconductors (ITRS) there are many challenges to be addressed to the increased scaling of bulk CMOS include Short Channel Effects (SCE's), such as sub-threshold leakage, Drain Induced Barrier Lowering (DIBL) and gate-dielectric leakage etc. The system reliability and system performance are affected due to challenges of CMOS scaling.

Many Researchers and scientists are working on CMOS scaling and alternate material ideas of semiconductors to overcome the above said challenges and trying to serve all the purposes of electronics and computer age. We have novel devices called FinFETs which are double-gate field-effect transistors and are capable of overcoming the scaling obstacles [1,2]. One of the most important features of FinFETs is that the front and back gates helps in effective controlling the electron flow through the channel hence reduce the short channel effects [3-4].FinFET technology is strong candidate for future Nano electronics due to its high-performance, low power consumption, reduced susceptibility to process variations, and ease of manufacturing using current processes.

The performance of SRAM subsystem is determined primarily by the delay involved in driving large loads on the bit line and the word line. Due to the large size of the on chip SRAMs in microprocessors designed in nanometer nodes,

leakage current is the major contributor to the total power dissipation in SRAMs. The exponential increase in leakage current results in large standby power. Increased transistor leakage and parameter variation present challenges for scaling of conventional six-transistor (6-T) SRAM cells [5, 6]. The SRAM array parametric standby leakage contributors include well isolation leakage [7, 8], subthreshold device leakage [9] and gate-oxide tunneling current [10, 11]. The major concern in future SRAMs is the leakage power consumption. Due to the reduced threshold voltage in future technologies, leakage power is increasing rapidly. Different SRAM cell designs have been proposed to target leakage control [12–13].

FinFET based SRAM's immunity to mismatch induced by process variation becomes quite imperative. Although there are some reports on the impact of parameter fluctuations in FinFETs by direct measurement [14, 15], the sensitivity of FinFET SRAM's stability to process variation and methods to enhance such stability have not yet been systematically addressed to the best of our knowledge. A FinFET uses an intrinsic body. It greatly suppresses the device-performance variability caused by the fluctuation in the number of dopant ions, while a planar-bulk MOSFET requires a heavily doped channel which causes serious process variability. It is preferable to extend the 6-transistor SRAM ability by effectively taking advantage of the FinFET-based technology together with the novel circuit technique. Increased process variation in short channel transistors is reducing the robustness of bulk Fin based SRAM. FinFET based SRAM design has been proposed as an alternative solution to the bulk devices. This also results in reduced stability of SRAM cell. FinFET is suitable for future nanoscale memory circuits design due to its reduced Short Channel Effects (SCE) and leakage current. In this chapter, the analysis of Static Noise Margin (SNM), Read Noise Margin (RNM), Write Noise Margin (WNM) and static power with variation of width of access, load and driver transistor have been carried out for the stability of FinFET based SRAM cell. HSPICE simulation results have been presented for the SNM, RNM and WNM.

II. FinFET

The FINFET based transistors offers good tradeoff for power as well offering interesting delay.Fig 1 shows a simple structure of FinFET, it is a 4 terminal device comprising of source and drain connected by a channel, the channel is wrapped around by multiple gates, in this case we consider 2 gates namely forward and backward gates or front and back gates. A FinFET is like a FET, but the channel has been "turned on its edge" and made to stand up hence structure gave the name for the device as FinFET. FinFETs may be substituted into a former bulk-CMOS design by merely shorting the front- and back-gates together during device fabrication to allow only one gate connection per FinFET. This transistor configuration is often called shorted gate (SG).

The device parameters considerations are one of the important steps in developing a spice model and then simulating it. Commonly used FinFET simulation models available to the research community are the Predictive Technology Model (PTM)[14] and BSIM-CMG/BSIM-IMG[15].

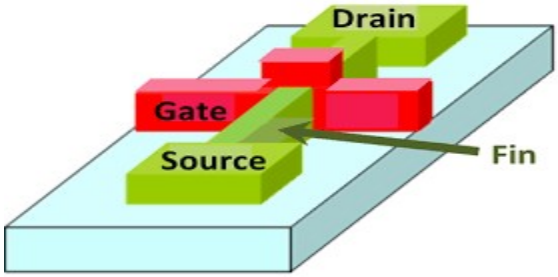

Fig.1FinFET

III. SRAM CELL

The static random-access memories (SRAM) are most widely used, due to their high performance: microprocessors may contain up to 70% of SRAMs in transistor count or area[2]. The trend in the semiconductor market is to push for more integration and more size reduction: the development and optimization of a technological node is more and more difficult and expensive. The reduction in size of a SRAM circuit in coming nodes is nonetheless complex and it faces several limitations. The reliability of the SRAM bit-cell is degraded with ever smaller technologies and the device functionality is endangered. Designing SRAM circuits in CMOS 45nm requires technical and technological solutions to overcome the size reduction limitations, while insuring satisfactory functionality, with a guaranteed reliability so that it can be economically fabricated

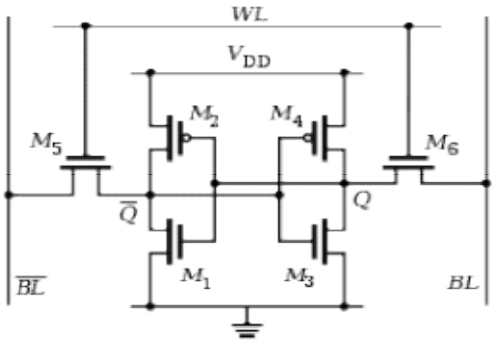

Fig. 2 6T SRAM Cell

IV. FinFET BASED SRAM CELL

The data storage cell, i.e., the 1-bit memory cell in static RAM arrays, invariably consists of a simple latch circuit with two stable operating points (states). Depending on the preserved state of the two-inverter latch circuit, the data being held in the memory cell will be interpreted either as a logic "0" or as a logic "1" .To access (read and write) the data contained in the memory cell via the bit line, we need at least one switch, which is controlled by the corresponding word line, i.e., the row address selection signal usually, two complementary access switches consisting of nMOS pass transistors are implemented to connect the 1-bit SRAM cell to the complementary bit lines (columns). This can be likened toturning the car steering wheel with both left and right hands in complementary directions.

The circuit structure of the full FinFET static RAM cell is shown in Figure 3, along with the pFET column pull-up transistors on the complementary bit lines. The most important advantage of this circuit topology is that the static power dissipation is even smaller; essentially, it is limited by the leakage current of the pFET transistors. A FinFET memory cell thus draws current from the power supply only during a switching transition. The low standby power consumption has certainly been a driving force for the increasing prominence of FinFET SRAMs.

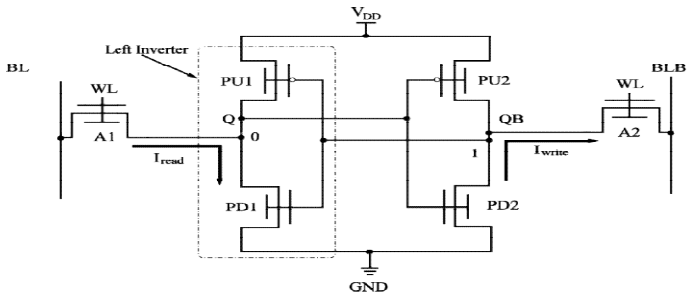

Fig. 3 FinFET Based SRAM Cell

V. PERFORMANCE MATRIC OF FinFET BASED SRAM CELL

A. Static Noise Margin

Stability, the immunity of the cell to flip during a read operation, is characterized by Static Noise Margin (SNM). SNM is calculated by the side of the largest square inside the FinFET based SRAM cross-coupled inverter characteristic measured during the read condition (BL 5 BL' 5 VD, and WL 5 VD) [18]. Static Noise Margin is the standard metric to measure the stability in SRAM bitcells. The SNM depends on the choice of the Vth for the FinFET's used in the SRAM cells. A high Vth means that drive current of these devices is small making the write operation more difficult, thus, increasing the SNM. One approach to achieve a low power cell with high stability is to use high Vth devices at the cost of performance. FinFETs provide a high drive current even with larger Vth, thereby, achieving high noise margins along with good write stability [19]. The SNM is seen to be the most sensitive to threshold voltage fluctuations in the access and pull-down nFinFETs and least sensitive to the fluctuations in the pull-up FinFET device. For FinFETs, the effect of Lg variation on Vth is small, so the effect on the SNM is also small.

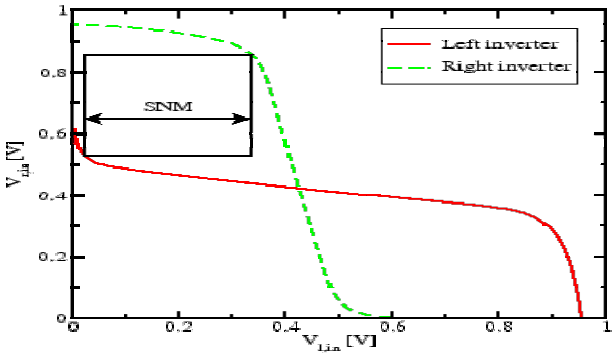

Fig. 4 SNM of 6T SRAM Cell

B. Read Noise Margin

RNM is often used as the measure of the robustness of an SRAM cell against flipping during read operation [20]. For read stability (High RNM) of FinFET based SRAM cell, pull down FinFET is typically stronger than access FinFET. The read margin can be increased by upsizing the pull-down transistor i.enFinFET, which results in an area penalty and/or increasing the gate length of the access FinFET increasing the 'WL' delay and hurting the write margin. A careful sizing of the Fin-FET device is required to avoid accidentally writing a 1 into the cell while trying to read a stored "0", thus, resulting in a read upset. The ratio of the widths of the pull-down FinFET to the access FinFET commonly referred to as the cell ratio (CR) determines how high the "0" storage node rises during a read access [19]. The Cell Ratio (CR) 5 (W1/L1)/(W5/L5) is as shown in figure 2. Smaller cell ratios translate into a bigger voltage drop across the pull-down FinFET requiring a smallernoise voltage at the "0" node to trip the cell. During a read operation, the conducting access FinFET lies inparallel to the pull-up PMOS, lowering the gain of the static transfer characteristic and further decreasing cell immunity to noise.

C. Write Noise Margin

Write Noise Margin (WNM) is the maximum bitline (BL) voltage that is able to flip the state of the FinFET based SRAM cell while bitline bar (BL') voltage is kept high [19]. Higher the WNM, greater is the stability. Use of a weaker pull up (pFinFET) and a stronger access FinFET helps the node storing "1" to discharge faster, thus facilitating a quicker write of "0". The write margin can be measured as the maximum BL' voltage that is able to flip the cell state while BL is kept high. Hence, the write margin improves with a strong access and a weak pull up FinFET at the cost of cell area and the cell read margin.

D. Power and Delay

Power dissipation of the FinFET SRAM cell assesses the utility of the cell in portable devices. The fundamental advantage of the FinFET based SRAM is in its low access time and power dissipation due to low SCE's and leakage current in FinFET device. While a strong driving current reduces the access time, it also increases the power dissipation in the SRAM cell. In SRAM, the propagation delay depends on the column height andwire delays. Thus segmentation is

employed to reducethe delay. Since the power-delay-product is constant for a device, increasing one decreases the other and vice-versa. Upsizing the FinFET device in SRAM cell decreases the delay at the cost of slightly increased power dissipation. However to reduce power dissipation, leakage currents need to be minimized which warrant an increase in the channel length or higher transistor threshold voltages. Larger channel length results in higher delay and there exists a trade-off between these two performance indices.

VI. MONTE CARLO ANALYSIS OF FinFET PROCESS VARIATION

The reason behind the observed random distribution of FinFET device parameters is due to the limited resolution of the photolithographic process which causes W/L variations in MOS transistors. The variations in W and L are not correlated because W is determined in the field oxide step while L is defined in the poly and source/drain diffusion steps. In FinFET based SRAM, the process parameters variation includeFinFET width (Wfin), fin thickness (Tfin) and threshold voltage (Vth). These variations affect the noise margins, power consumption and delay. Memory designs are optimized for 6s variations [20]. To assess the impact of process parameters on FinFET SRAM, we carried out Monte Carlo simulationson HSPICE.

VII. RESULT AND DISCUSSION

It can be seen that the high Static Noise Margin (SNM) reduces and low SNM increases with decrease in the width of loadFinFET M2. Thus, as width of the load FinFET reduces, so does the driving capability of the load device. This implies that Q reaches to VOH at a much higher voltage, thus, resulting in a decrease in high SNM. It is further observed that as the widths of the pull-up device decreases, the switching threshold also tends to reduce. Since the driving capability of M2 reduces with the reduction in width, therefore, it requires lesser amount of voltage at BL' for the purpose of switching threshold.The variation of Static Noise Margin (SNM) for driver FinFET M1 with variation of its width is increase in the width of driver FinFET M1, the high SNM reduces and low SNM increases. This is due the fact that the leakage current is considerably reduced due to increased controlof the FinFET device structure, resulting relatively in high Ion/Ioff ratio. In the case of RNM, the stability of the cell is most seriously compromised as the node containing '0' is pulled up to a voltage determined by the relative sizing of driver and access FinFET's.

	Load	**Driver**	**Access**	**All W**
Mean(mV)	27.1390	27.1460	27.6201	28.0672
Stander Deviation (mV)	1.0501	1.0030	2.0875	2.9062

Table. 1 Mean and Standard deviation of RNM Monte Carlo analysis

	Driver	**Load**	**Access**	**All W**
Mean(mV)	81.5366	81.5047	81.7485	65.6410
Standard Deviation	1.9654	2.4564	4.8751	4.9858

(mV)				

Table. 2 Mean and Standard deviation of WNM Monte Carlo analysis

VIII. CONCLUSION

In this paper, we have analyzed different tradeoffs involved in the design of FinFET based SRAM and optimized the performance of the cell for robustness. The analysis of SNM, RNM, WNMload and driver have been carried out. Further, the effect of process variation on the SRAM cell performance was analyzed using Monte Carlo simulation on HSPICE. It was identified that while the relative levels of the noise margins were lower for the underlapped case, the standard deviation was considerably lower too. It was also found that smaller FinFET widths give rise tolarger deviations than larger ones. Thus in future FinFET SRAM based on minimum FinFET width, would be prone to process variations. The temperature dependence of noise margins and static power was also observed for FinFET based SRAM. While SNM and RNM decreased with increasing temperature, WNM increased. Since the stability of the FinFET based SRAM cell in the idle state is the most important metric, temperature effects have to be accounted for in design of memory circuits.

REFERENCES

[1] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur and H.-S . P. Wong, Mar. 2001."Device scaling limits of Si MOSFETs and their application dependencies," Proc. of the IEEE, vol. 89, no. 3, pp. 259-288.

[2] T.-J. King, Nov. 2005. "FinFETs for nanoscale CMOSdigital integrated circuits," in Proc. Int. Conf. Computer - Aided Design, pp. 207-210.

[3] J.-P. Colinge, 2008, "The SOI MOSFET: From single gate to multigate," `in FinFETs and Other Multi-Gate Transistors, 1st ed., J.-P. Colinge, Ed., New York, Springer, , pp. 1-48.

[4] Nirmal, Vijayakumar and Sam Jabaraj (2010), Nand Gate using FINFET for Nano-Scale Technology, In International Journal of Engineering Science and Technology, Vol. 2(5), pp-1351-1358.

[5] Z. Guo, S. Balasubramanian, R. Zlatanovici, T. J. King, and B. Nikolic, “FinFET based SRAM design,” in Proc. Int. Symp. Low Power Electronics and Design (ISLPED), 2005, pp. 2–7.

[6] C. Hyung, I. Kim, and J. J. Kim, “A forward body-biased low-leakage SRAM cache device, circuit and architecture considerations,” IEEE Trans. VLSI Syst., vol. 13, no. 3, pp. 349–357, 2005.

[7] H. Pilo, “SRAM design in the nanoscale era,” in Proc. Int. Solid State Circuits Conf., 2005, pp. 366–367.

[8] H. Qin, Y. Cao, D. Markovic, A. Vladimirescu, and J. Rabaey, “SRAM leakage suppression by minimizing standby supply voltage,” in Proc.5th Int. Symp. Quality Electronic Design, 2004, pp. 55–60.

[9] J. H. Choi, A. Bansal, M. Meterelliyoz, J. Murthy, and K. Roy, “Leakage power dependent temperature estimation to predict thermal runawayin FinFET circuits,” in IEEE Proc. Int. Conf. Computer Aided Design (ICCAD), Nov. 5–9, 2006, pp. 583–586.

[10] Wang and B. K. James, “A novel two-port 6T CMOS SRAM cell structure for low voltage VLSI SRAM with single-bit-line simultaneous readand write access (SBLSRWA) capability,” in Proc. IEEE Int. Symp. (ISCAS), 2000, pp. 733–736.

[11] W. Hu, X. Chen, X. Zhou, Z. Quan, and L. Wei, "Quantum-mechanical effects and gate leakage current of nanoscale n-type fi nFETs: A 2D simulation study," Microelectron. J., vol. 37, pp. 613–619, 2006.

[12] S. Ohbayashi, "A study of fanout optimization of SRAM decoder with a line capacitance," Trans. IEICE, vol. E-73, no. 11, pp. 1855–1857, Nov. 1990.

[13] T. Miwa, J. Yamada, and H. Koike, "A 512 Kbit low voltage NV-SRAM with the size of a conventional SRAM," in Symp. VLSl Circuits Dig., 2000, pp. 129–132.

[14] J. Bhavnagarwala, T. Xinghai, and J. D. Meindl, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 658–665, Apr. 2001.

[15] B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C. Y. Yang, C. Tabery, C. Ho, Q. Xiang, T. J. King, J. Bokor, C. Hu, M. R. Lin, and D. Kyser, "FinFETscaling to 10 nm gate length," in IEDMTech. Dig., 2002, pp. 251–254.

[16] W. Zhao and Y. Cao, May 2006, "New generation of predictive technology model for sub-45nm design exploration," in Proc. Int. Symp. Quality of Electronic Design,pp. 585-590.

[17] M.V.Dunga, C.-H. Lin, A. M. Niknejad and C. Hu, 2008 "BSIM-CMG: A compact model for multi-gate transistors," in FinFETs and Other Multi-Gate Transistors,1st ed.,J.-P. Coligne, Ed., New York, Springer, pp. 113-153.

[18] Darsen D. Lu, Chung-Hsun Lin, Ali M. Niknejad and Chenming Hu 2010. "Compact Modeling of Variation in FinFET SRAM Cells" IEEE Design and Test of computer.

[19] J. Yang and S. Balasubramanium, "Design of sub-50 nm FinFET based low power SRAMs," Semicond. Sci. Technol., vol. 23, p. 13, 2008.

[20] Rashmi, A. Kranti, and G. A. Armstrong, "6-T SRAM cell design with nanoscale double-gate SOI MOSFETs: Impact of source/drain engineeringand circuit topology," Semicond. Sci.Technol., p. 13, 2008.

[21] E. Chin, M. Dunga, and B. Nikolic, "Design trade-offs of a 6T FinFET SRAM cell in the presence of variations," in Proc. IEEE Symp. VLSI Circuits,2006, pp. 445–449.