Comparative Analysis of 28T Full Adder with 14T Full Adder using 180nm

Arvind Nigam,
M.Tech. Scholar, Rama University, Kanpur
arvind_nigam@rediffmail.com

Raghvendra Singh,
Dept. of ECE, Rama University, Kanpur
raghav.raghvendra7@gmail.com

***Abstract*— Full adder is the basic block of arithmetic circuit found in microcontroller and microprocessor inside arithmetic and logic unit (ALU). Improvement of the adder is thus essential for upgrade the performance of those circuits where adder is employed. Full adders, till now, have been designed using wide range of structures for improvement of various parameters like power consumption, speed performance and structure size. This paper described a comparative analysis of 28T and 14T full adder with the aim of increasing power efficiency and reducing structure size at 180nm technology. In this paper, the simulation results have been obtained for power by varying different parameters of the designed circuit using 180nm technology with Empyrean Aether.**

Keywords- Full Adder, Low Power, Cache Memory, Arithmetic Operation, Leakage Power

I. INTRODUCTION

Full adders have been utilized as a base circuit in various arithmetic circuits to carry out arithmetic operations like addition, subtraction, multiplication, address calculation and MAC unit etc. [2]. Apart from arithmetic operations, adders are utilized to generate memory locations in different architectures of microprocessors and cache memories. Thus improvement in the full adder would prove more beneficial for all the circuits where its application has a significant effect in the performance of the circuit where it has been employed. The most important parameters to be kept in consideration are compactness and power which affects the performance and usefulness of any VLSI circuit. The paper here aims at analysis and improvement of power efficiency and structure size reduction of the 28T full adder at 180nm technology. As compared to conventional structure, 14T structure saves up to 78% of the number of transistors involved in the conventional full adder and so the area overhead [16] [19] is reduced. We have started with the most conventional 28 transistor full adder and then studied full adders consisting of as less as 14 transistors (14T).

The power consumption for CMOS circuits [13] [20] is described by the following equation:

$$P_{avg} = P_{dynamic} + P_{short-circuit} + P_{Leak}$$

$$P = fCVdd^2 + fI_{short}V_{dd} + I_{leak}V_{dd} \quad (1)$$

We clearly see that the power depends on different parameters as well as on supply voltage (V_{dd}). Lowering V_{dd} would significantly reduce the power consumption of the circuit. This basic concept would be utilized to improve the power performance of the adder in this paper.

II. FULL ADDER

Full adder is a combinational circuit that performs the addition operation of 3 input bits. It basically consists three inputs and two outputs. The input variables are expressed by A, B and Cin. The two output variables are expressed by sum (S) and carry (Cout) [4]. Fig. 1 shows the essential block diagram of full adder cell. The Boolean expression for full adder operation is defined below:

SUM = ((A⊕B)⊕Cin) (2)
Cout =AB + (A⊕B)Cin (3)

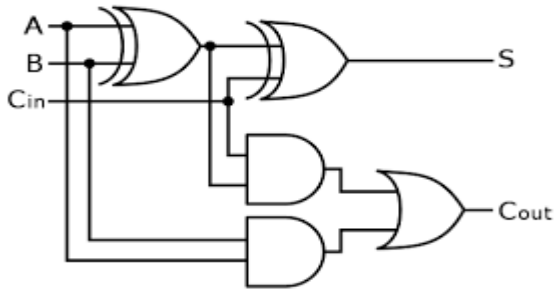


Fig.1. Logic Diagram of basic Full Adder circuit

TABLE I TRUTH TABLE FULL ADDER

A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

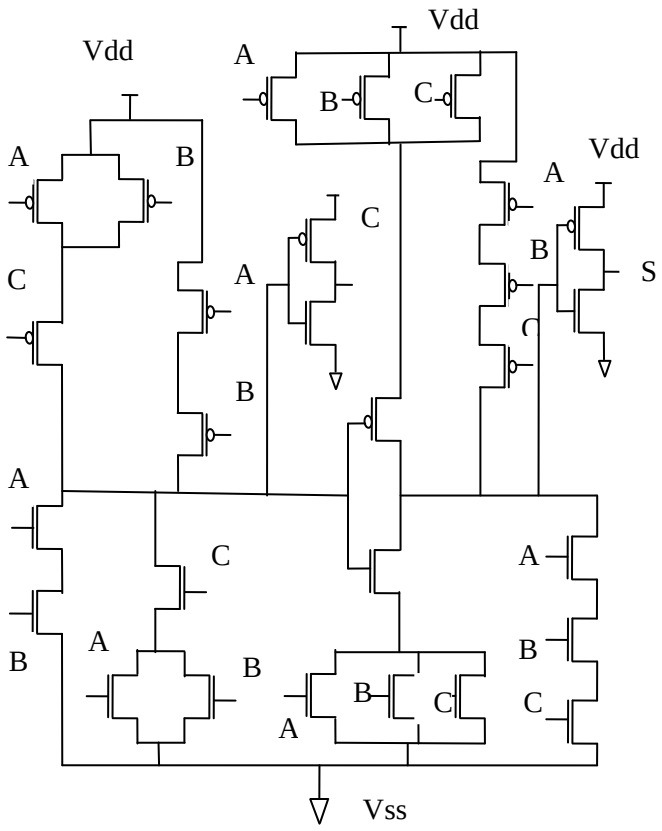


Fig.2. Schematic of 28T Full Adder

III. 28T FULL ADDER CIRCUIT

The 1-bit conventional CMOS full adder cell is shown in Fig2. The 1-bit full adder cell has 28 transistors. The CMOS design style is not area efficient for complex gates with large fan-ins. Thus, care must be taken when a static logic style is selected to realize a logic function. The pseudo NMOS technique is straight forward. The pass transistor logic style is known to be a popular method for implementing some specific circuits such as multiplexers and XOR -based circuits, like adders. A classical design of standard static CMOS full adder is based on regular CMOS structure with conventional pull-up and pull-down transistor providing full -swing output and good driving capabilities.

IV. 14T FULL ADDER CIRCUIT

To reduce the number of transistors in the traditional full adder, XOR and XNOR circuits based on the pass transistor logic were used which results in the design of 14T full adder [5] as shown in fig.3. The development of the 14T full adder led to better results for delay as well as power consumption as compared to the previous works in the full adder. 14T full adder worked well with high performance multipliers with less power dissipation. However the adder did not showed improvement in threshold power loss. More over the 14T adder would consume significant power as compared to the presented 28T full adder. The 14T adder with 14 transistors consumes considerably less power in the order of microwatts and has higher speed. The 14T adder reduces threshold loss problem compared to the 28 transistor adders. In this section single bit full adder circuit is designed by using MOSFET for improve the performance of adder in terms of power and leakage using 14 transistors. This cell is constructed by using the 4T XOR gate. It is the essential element of full adder cell and it generates the basic addition operation of adder cell. It behaves like a single half adder cell. In the 14T full adder cell we used two 4T XOR gate. Conventionally XOR gate use 8 MOSFETs for proper working, but present we have different topologies. Here we have used 4T XOR gate to increase circuit density [11] [12]. Using this XOR gate, reduction in size of full adder is achieved and overall leakage is also reduced. Output waveform of 14T full adder is shown in fig.4.

The 14T full adder contains a 4T PTL XOR gate, shown in Figure, an inverter and two transmission gates based multiplexer designs for sum and Cout signals[9]. This circuit has 4 transistors XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously to generate Sum and Cout. It is a faster adder. The circuit is simpler than the conventional adder. The power dissipation in

this circuit is more than the 28T adder. However with same power consumption it performs faster [7].

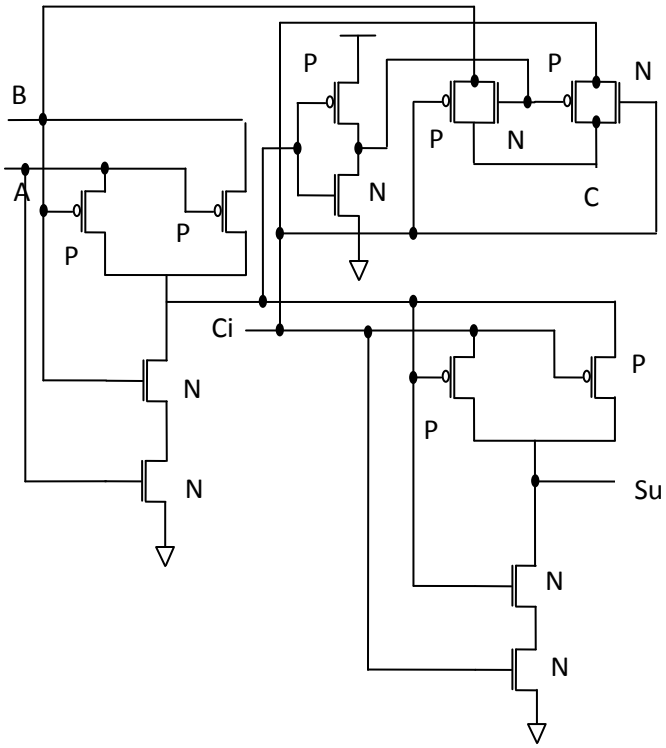


Fig.3: Schematic of 14T Full Adder

V. 4T XOR Gate

The basic element used in the full adder design is the XOR gate which generates basic addition operation in the adder circuits. A single XOR generates simple two bit addition i.e. it behalves like a single half adder. The XOR gate conventionally uses 8 MOSFETs for proper working, however, at present we have different XOR gate topologies [3] [4].

However in this paper, we have used 4T XOR gate to get proper response and to attain increased circuit density. Figure 4 show the schematic and of 4T XOR gate. Application of this XOR gate would now provide significant reduction in size of full adder thus increasing the circuit density and reducing the overall leakage.

TABLE II: TRUTH TABLE OF XOR GATE.

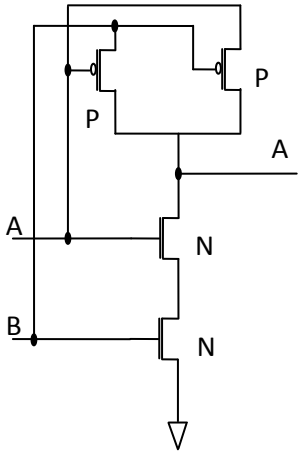


Fig. 4: 4T XOR Gate Schematic.

VI. PERFORMANCE ANALYSIS AND SIMULATION RESULT

The power waveform of 28T full adder signifies the power consumed by the circuit over the period of simulation, obtained by the Empyrean Aether tools. The average power [13] [14] over this simulation has been indicated on the waveform which needs to be improved.

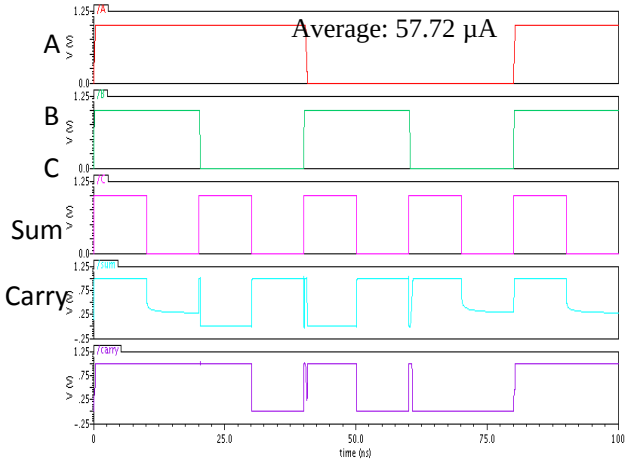
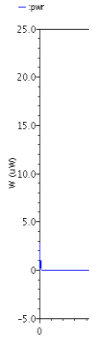


Fig. 5 (a) 28T Full Adder Output waveform



A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

Fig. 5 (b): 28T Full Adder Power waveform.

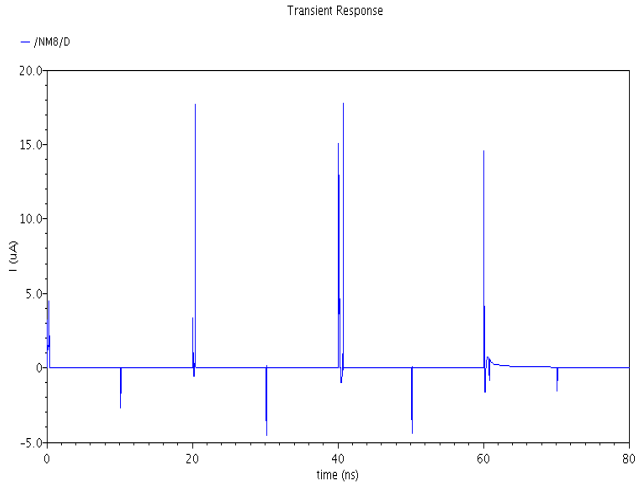


Fig. 6: Leakage current waveform of 28T full adder.

The leakage current contributes the amount of leakage power in the CMOS circuit. More is the leakage current more will be the leakage power which must be lowered in order to make the circuit more power efficient. The amount of leakage current here is result of integration of leakages due to individual transistors. Hence it may be concluded that if number of transistors is reduced the leakage would be less. Further, as described in equation 1, it may be noted that on reducing the supply voltage, which results in reduction of leakage current as well, would reduce the power consumption to a significant level.

The full adder shown here has been analyzed for different parameters later in this paper. The 28T full adder presented in this paper, shows optimized results in power and delay. The design also uncovers performance improvement as compared to the SERF 28T adder [7]. The width by length ratio (W/L) for all nMOS transistors is 1/1 and for pMOS transistors is 2.5/1.

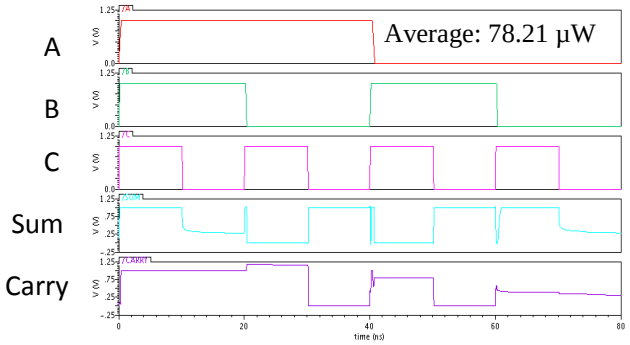


Fig. 7 (a) . 14T Full Adder Output waveform

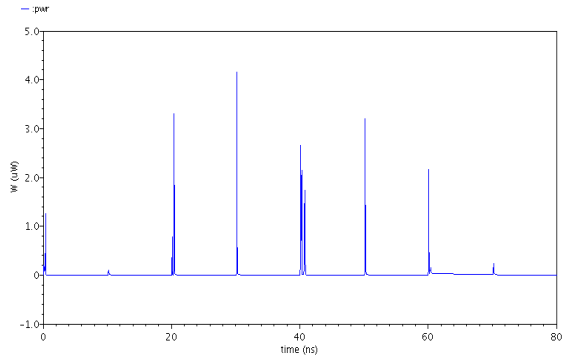


Fig. 7 (b) 14T Full Adder Power waveform.

The output waveform of 14T adder clearly verifies the operation of the full adder. Result of transient simulation shows that the power consumed by the circuit is limited to 38.4 nW at a supply voltage of 1 V which is much less as compared to the 28T adder at 180 nm technology.

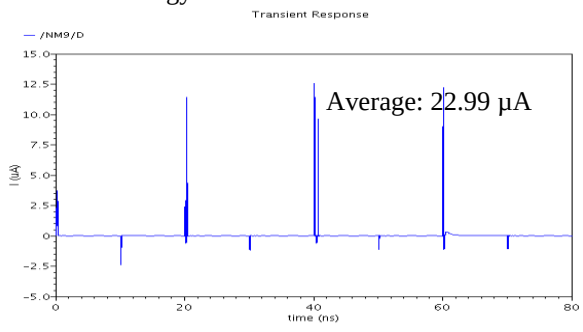


Fig.8. Leakage current waveform of 14T full adder

VII. COMPARATIVE RESULTS OF 14T AND 28T FULL ADDER

The 14T and 28T Full adders have been simulated using the Empyrean Aether tool simulator. The resulting waveform of power clearly indicates that the 14T full adder show improved performance over the 28T full adder in terms of power consumption. The comparison of different parameters of the two adders at 180 nm technology has been tabulated in table III.

TABLE III

.Sr. No.	Parameter	28T Adder	14T Adder	14T Adder
1	Technology	180 nm	180 nm	180 nm
2	Supply	1 V	1 V	0.7
3	Power	78.21 µW	38.4 µW	21.04 µW
4	Reduction in structure size	69%	78%	78%

Table III: Comparative analysis table of 14T and 28T Full Adder.

The summarized results signify that 14T full adder shows better performance as compared to 28T full adder. Reducing the number of transistors resulted in significant amount of reduction in leakage. Further, reduction in supply voltage made the power consumption much lower.

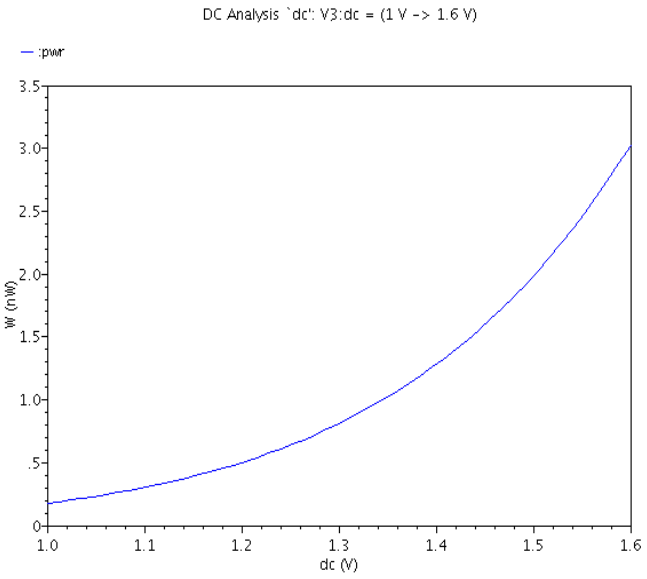


Fig. 9 (a) Power Versus Vdd curve for 28T Full Adder

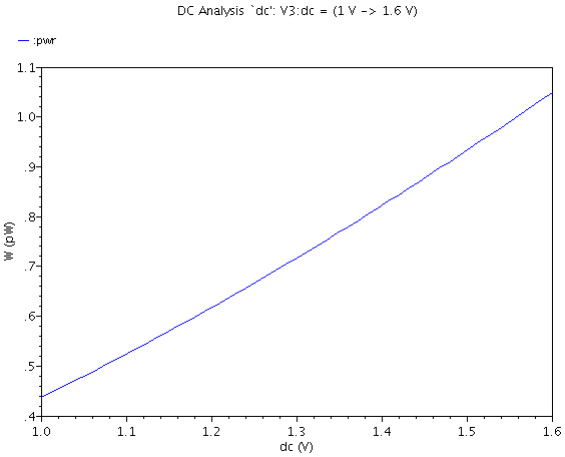


Fig. 9(b). Power Versus Vdd curve for 14T Full Adder.

Comparison of both adder topologies in terms of power consumption can be seen on power versus Vdd curve. The curve signifies that as the Vdd (supply) increases power increases as a function of Vdd. In 28T adder power varies as exponential function of Vdd in the range of micro-watt. However in 14T curve advances much as linear function of Vdd in the range of nano-watt. This makes clear that the power consumption of 14T is much improved even at increased supply voltages.

VIII. CONCLUSION

The analysis in this paper has been carried out while analyzing both 14T and 28T full adders individually and comparing them on the basis of calculation of power by varying different parameters. The results show that 14T full adder has proved to be a better option as compared to 28T full adder, mostly in terms of power consumption. From the power –Vdd curve we observe that at 1.6 V, 28T adder consumes about 3 µW, while 14T consumes only 1.5 nW. Thus 14T consumes 10^3 times less power than the power consumed by 28T full adder.

ACKNOWLEDGMENT

The endeavour in this paper was supported by Rama University, Kanpur, India

REFERENCES

[1] Tripti Sharma, K.G.Sharma, Prof.B.P.Singh, "High Performance Full Adder Cell: A Comparative Analysis", Proceedings of 2010 IEEE Students' Technology Symposium, IIT Kharagpur, 3-4 April 2010.

[2] V. Vijay, J. Prathiba, S. Niranjan Reddy and P. Praveen Kumar, "A Review Of The 0.09 um Standard Full Adders", International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.3, June 2012.

[3] Phuong Thi Yen, Noor Faizah Zainul Abidin, Azrul Bin Ghazali, "Performance Analysis Of, Full Adder (Fa) Cells", IEEE Symposium on Computers & Informatics, 2011.

[4] G.Shyam Kishore, Associate.Prof, ECE dept, JITS, Karimnagar, Andhra Pradesh, India, "A Novel Full Adder with High Speed Low Area", Proceedings published in International Journal of Computer Applications® (IJCA) , 2nd National Conference on Information and Communication Technology (NCICT) 2011.

[5] Tripti Sharma, Prof.B.P.Singh, K.G.Sharma, Neha Arora Electronics & Communication Deptt. MITS Deemed University, Rajasthan INDIA, "High Speed, Low Power 8T Full Adder Cell with 45% Improvement in Threshold Loss Problem", Recent Advances in Networking, VLSI and Signal Processing.

[6] Dr.P.T. Vanathi, Dr.J. Ramesh, K. Revathy, R. Preethi, C. Haritha Laxmi and K. Keerthana, "Performance Analysis of High Performance Adder Architectures", Bonfring International Journal of Power Systems and Integrated Circuits, Vol. 2, Special Issue 1, Part 2, February 2012.

[7] Farshad Moradi, Dag.T. Wisland, Hamid Mahmoodi, Snorre Aunet,Tuan Vu Cao, Ali Peiravi, "Ultra Low Power Full Adder Topologies", 2009 IEEE.

[8] Massimo Alioto, Member, IEEE, and Gaetano Palumbo, Senior Member, IEEE, "Analysis and Comparison on Full Adder Block in Submicron Technology", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, VOL. 10, NO. 6, December 2002.

[9] Amin Bazzazi, Member, IAENG, Alireza Mahini and Jelveh Jelini, "Low Power Full Adder Using 8T Structure", Proceedings of the International MultiConference of Engineers and Computer Scientist, HongKong, Vol II, IMECS 2012, March 14 – 16, 2012,.

[10] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha and Jin-Gung Chung, "Low Power Full Adder Using 8T Structure", IEEE Transactions on Circuits and Systems – II: Express Briefs, Vol.51, No.7, July 2004.

[11] Po-Ming Lee, Chia-Hao Hsu, and Yun-Hsiun Hung Dept. of Electronics Engineering, Southern Taiwan University of Technology, "Novel 10-T full adders realized by GDI structure", 2007 IEEE.

[12] M.Hosseinghadiry, H. Mohammadi, M.Nadisenejani, "Two New Low Power High Performance Full Adders with Minimum Gates", International Journal of Electrical and Computer Engineering, 4:10, 2009.

[12] M.Hosseinghadiry, H. Mohammadi, M.Nadisenejani, "Two New Low Power High Performance Full Adders with Minimum Gates", International Journal of Electrical and Computer Engineering, 4:10, 2009.

[13] Mohammad Hossein Moaiyeri and Reza Faghih Mirzaee, Keivan Navi, "Two New Low-Power and High-Performance Full Adders", Journal Of Computers, Vol. 4, No. 2, February 2009.

[14] Mariano Aguirre-Hernandez and Monico Linares-Aranda, "CMOS Full-Adders for Energy-Efficient Arithmetic Applications", IEEE Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 19, No. 4, April 2011.

[15] Walid Ibrahim, Senior Member, IEEE, and Valeriu Beiu, Senior Member, IEEE, "Threshold Voltage Variations Make Full Adders Reliabilities Similar", IEEE Transactions On Nanotechnology, Vol. 9, No. 6, November 2010.

[16] Deepa Sinha, Tripti Sharma, K.G.Sharma, Prof.B.P.Singh, "Design and Analysis of Low Power 1-bit Full Adder Cell", IEEE, 2011.

[17] Phuong Thi Yen, Noor Faizah Zainul Abidin, Azrul Bin Ghazali, "Performance Analysis Of Full Adder (FA) Cells", IEEE Symposium on Computers & Informatics, 2011.

[18] Mallikarjuna Rao Nimmagadda, Ajit Pal, "Low-Power, Energy-Efficient Full Adder for Deep-Submicron Design", IEEE Computer Society Annual Symposium on VLSI, 2011.

[19] Walid Ibrahim, Azam Beg, and Valeriu Beiu, "Highly Reliable and Low-Power Full Adder Cell", 2011 11th IEEE International Conference on Nanotechnology Portland Marriott August 15-18, 2011.

[20] T. Vigneswaran, B. Mukundhan, and P. Subbarami Reddy, "A Novel Low Power, High Speed 14 Transistor CMOS Full Adder Cell with 50% Improvement in Threshold Loss Problem", World Academy of Science, Engineering and Technology 13, 2008.

[21] Dan Wang, Maofeng Yang, Wu Cheng, Xuguang Guan, Zhangming Zhu, Yintang Yang, "Novel Low Power Full Adder Cells in 180nm CMOS Technology", 4th IEEE Conference on Industrial Electronics and Applications, ICIEA 2009, pp 430-433.

[22] J. Wang, S. Fang, and W. Feng, ―New efficient designs for XOR and XNOR functions on the transistor level‖ , IEEE J. Solid-State Circuits, vol. 29, no. 7,Jul. 1994, pp. 780–786.

[23] R. Zimmermann and W. Fichter, ―Low –power logic styles: CMOS versus pass-transistor logic,‖ IEEE J. Solid-State Circuits, Vol. 32, July 1997,pp.1079-90

[24] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicron CMOS Circuits", Proceedings of the IEEE 2003, Vol. 91, No.2, pp. 305-327.

[25] Vahid Moalemi and Ali Afzali-Kusha, "Subthreshold1-bit Full adder cells in sub-100nm technologies", IEEE Computer Society Annual Symposium on VLSI (ISVLSI-07), Porto Alegre, Brazil, March 9-11, 2007 (ISBN 0-7695-2896-1).

[26] Dan Wang, Maofeng Yang, Wu Cheng, Xuguang Guan, Zhangming Zhu, Yintang Yang, "Novel Low Power Full Adder Cells in 180nm CMOS Technology", 4th IEEE Conference on Industrial Electronics and Applications, ICIEA 2009, pp 430-433.

[27] Shipra Mishra, Shelendra Singh Tomar and Shyam Akashe, "Design low power 10T full adder using process and circuit techniques", 7th IEEE International Conference on Intelligent Systems and Control(ISCO) Coimbatore 2013, pp. 325-328.