Leakage Current Reduction in Nanoscale Memories

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Abstract--- The power consumption of high performance integrated circuits has increased significantly with technology scaling. Higher power consumption shortens the battery lifetime of portable devices. Furthermore, the increased power consumption poses limitation on the continued technology scaling due to the associated higher power density. In this paper, the sources of power consumption are identified and modeled. Implementation of various techniques and the proposed technique for reducing total leakage current for low power SRAM cell is presented. It is observed in the paper that the total leakage current and power dissipation of the proposed technique is minimized to 68.15 fA and 8.78 nW respectively. Simulations have been performed on Cadence virtuoso 45 nm technologies.

Keywords: SRAM; FinFET; Leakage Current; Power Dissipation

I INTRODUCTION

Over the past three decades, scaling of Complementary metal-oxide-semiconductor (CMOS) technology has been a main key for continuous progress in silicon-based semiconductor industry. However, as the technology scaling enters nanometer regime (gate electrode reduced), CMOS devices are facing many serious problems because the gate starts losing control over the channel. These problems are such as increased leakage currents, difficulty on increase of on-current, large parameter variations, low reliability and yield, increase in manufacturing cost, and etc. To sustain the historical improvements, various innovations in CMOS materials and device structures have been researched and introduced. One such FinFET device structures have been introduced to overcome above mentioned serious problems which are faced by CMOS technology beyond 65nm. The FinFET devices are designed to address this performance shortcoming by wrapping the gate electrode around the channel, instead of having it laid on top of the channel.

The structure of a FinFET with a cut-plane view throughout the fin is shown in Figure 1. To make a double gate FinFET, the top oxide is made much thicker than the side oxides in order to effectively inactivate the top gate.

As is evident, the width of a triple-gate FinFET is $W = 2H_{fin} + W_{fin}$. In many cases, Wfin is small in order to have sufficiently small short channel effect. Moreover, in a DG FinFET, the top gate is ineffective. As a result, W is approximately $2H_{fin}$. As a result, the physics of a FinFET becomes largely similar to that of a DG MOSFET. Thus, almost all the literature that discusses compact model development for DG MOSFETs can be applied to FinFETs with a small parameter (H_{fin}) adjustment, as done in [1].

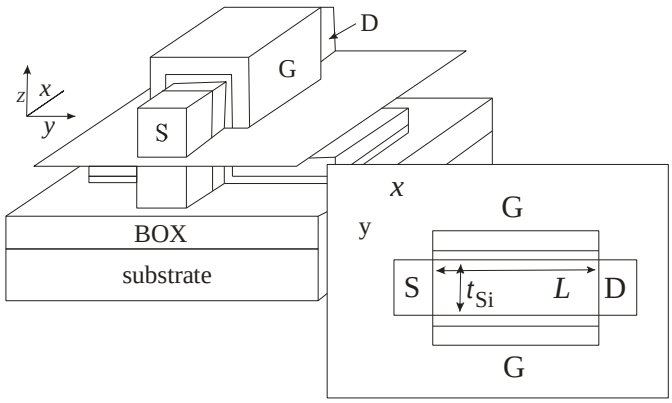

Fig. 1. 3D view of a FinFET with a cut-plane across the fin

The long narrow portion of the fin that is not under the gate, is called the extension region. This is a region that is technologically unavoidable, because it is not probable to have a steep lateral doping gradient, beginning from a highly doped source/drain, and ending with a lightly doped channel region (a lightly doped body is preferred because it helps reduce corner effects [2-4], random dopant fluctuations and mobility degradation effects). As a result, FinFETs typically have a relatively large parasitic series resistance.

II FINFET BASED 6T SRAM CELL

We need the proper optimization of the FinFETs to reduce leakage and improve stability in SRAM cell. To reduce the leakage in FinFET SRAM cells, proper optimization of supply voltage (VDD), fin height (H and threshold voltage (T is required to enhance the stability. Memories are required to have short access times, and low power dissipation, thus FinFET based SRAM cells are used. FinFET based SRAM cells are most popular due to the low power dissipation. FinFET based 6T SRAM cell structure is different from the conventional 6T SRAM cell. FinFETs replaces the bulk MOSFETs and this modification has been done in order to reduce the write access time. The FinFET based 6T SRAM cell consists of two FinFET based access transistors and the cross-coupled inverters as the basic memory element. The gates of the two access transistors are connected to the word-

line (wl) and source to bit line (wbl) and bit line bar (wblb) respectively. Whenever the memory element is to be accessed for read or write operation, the access transistors must be switched ON. The FinFET based 6T SRAM cell design is shown in Figure 2.

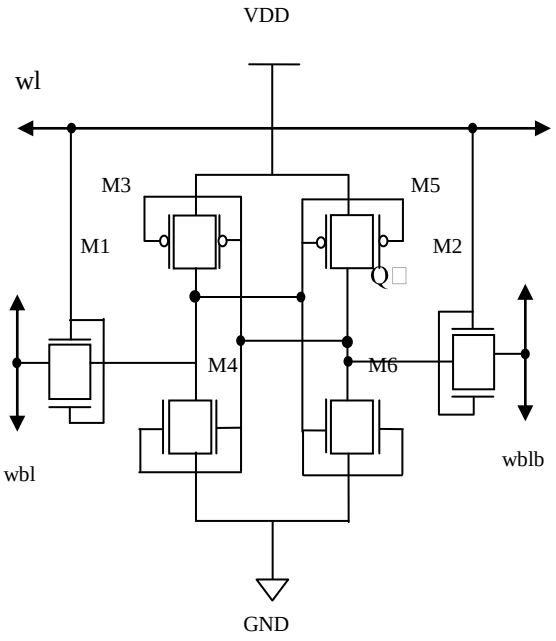

Fig. 2. FinFET based 6T SRAM cell

The parameters used to design and simulate the FinFET based SRAM cell at 45nm is shown in Table I.

TABLE I. PARAMETERS USED IN SIMULATION FOR 45 AND 32 NM TECHNOLOGY.

Parameters	Values
L_{eff}	45nm
T_{fin}	8.4nm
H_{fin}	60nm
t_{ox}	1.5nm
Channel doping	Intrinsic
N_{body}	$2\times10^{16}cm^{-3}$
$Vth_{o,n}$	0.31v
$Vth_{o,p}$	-0.25v

Leakage power waveform of conventional FinFET based 6T SRAM is shown in Figure 3 and Figure 4 respectively.

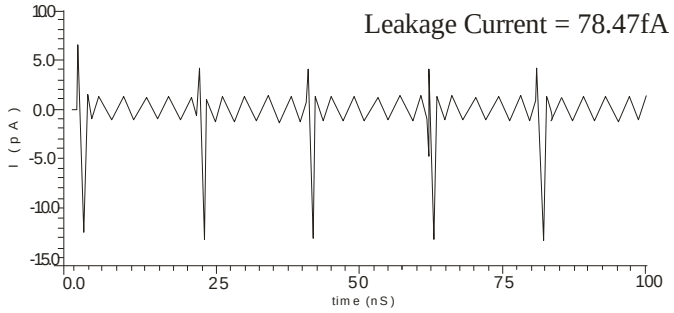

Fig. 3. Leakage Current of FinFET based 6T SRAM cell

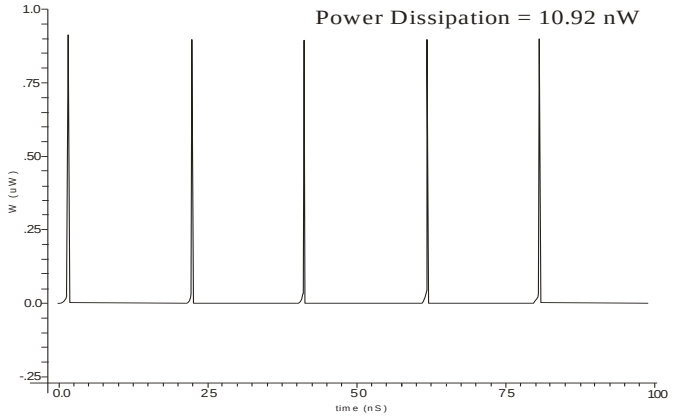

Fig. 4. Power Dissipation of FinFET based 6T SRAM cell

III DESIGN TECHNIQUES FOR REDUCING TOTAL LEAKAGE CURRENT FOR LOW POWER SRAM CELL

If the word line is not asserted, the access transistors M1 and M2 disconnect the cell from the bit lines. The two cross-coupled inverters formed by M3-M6 will continue to reinforce each other as long as they are connected to the supply. Thus in this mode, a large amount of power is consumed by SRAM in order to retain the data, so various techniques are suggested to reduce the power consumption of the circuit by reducing the leakage current.

A. Multi-threshold CMOS (MTCMOS)

Multi-threshold CMOS is a variation of CMOS chip technology which has transistors with multiple threshold voltages (Vth) in order to optimize delay or power. The Vth of a MOSFET is the gate voltage where an inversion layer forms at the interface between the insulating layer (oxide) and the substrate (body) of the transistor. Low Vth devices switch faster, and are therefore useful on critical delay paths to minimize clock periods. The penalty is that low Vth devices have substantially higher static leakage power. High Vth devices are used on non-critical paths to reduce static leakage power without incurring a delay penalty. Typical high Vth devices reduce static leakage by 10 times compared with low Vth devices [5].

In MTCMOS technique, transistors of low threshold voltage become disconnected from power supply by using high threshold sleep transistor on the top and bottom of the logic circuit. Transistor having low threshold voltage (low-Vth) is used to design logic as shown in Figure 5. The sleep transistors are controlled by the sleep signal. During the active mode, the sleep signal is disserted, causing both high Vth transistor to turn on and provide a virtual power and ground to the low Vth logic. When the circuit is in in-active mode, the sleep signal is asserted, forcing both high Vth transistor to cut-off and disconnect power lines from the low Vth logic. This results in a very low leakage current from power to ground in standby mode. Leakage current and Leakage power waveform of FinFET based 6T SRAM implemented using the MTCMOS technique is shown in Figure 6 and Figure 7 respectively.

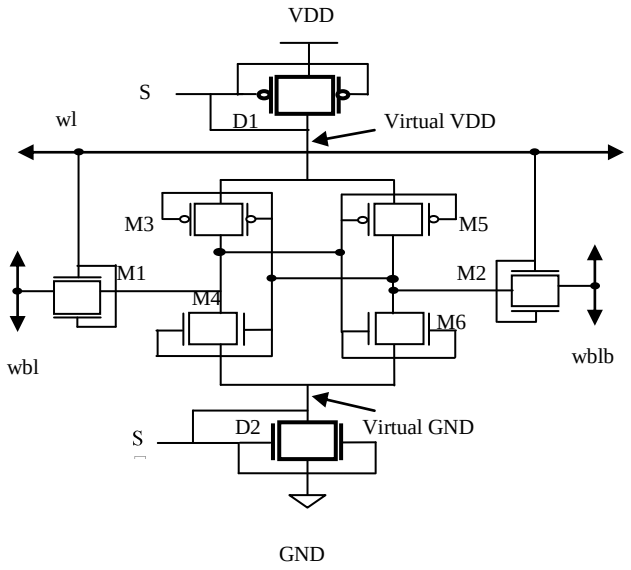

Fig. 5. Implementation of MTCMOS technique on FinFET based 6T SRAM cell

One drawback of MTCMOS technique is the portioning and sizing of sleep transistors is difficult for large circuits.

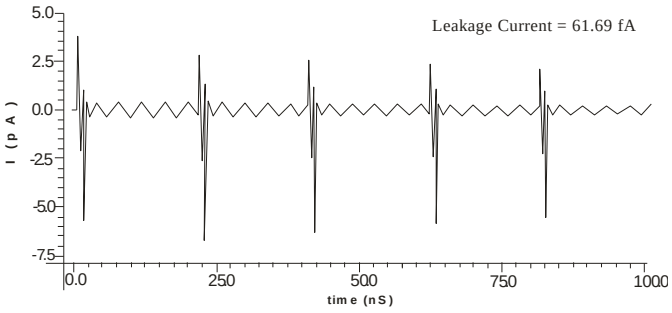

Fig. 6. Leakage current waveform after implementation of the MTCMOS technique on FinFET based 6T SRAM cell

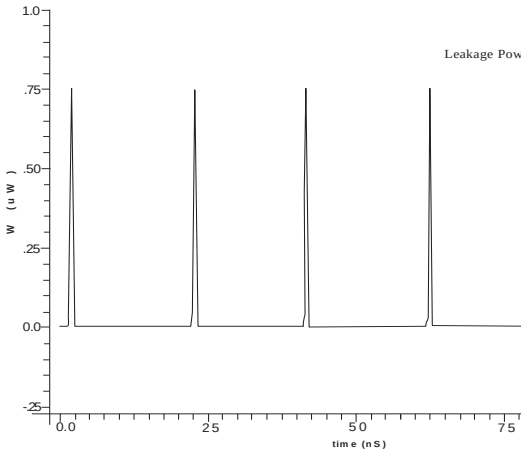

Fig. 7. Leakage power waveform after implementation of the MTCMOS technique on FinFET based 6T SRAM cell

B. Self Controllable Voltage Level Technique (SVL)

Self controllable voltage technique is applied on the shorted gate DG FinFET SRAM cell to reduce the leakage in the cell.

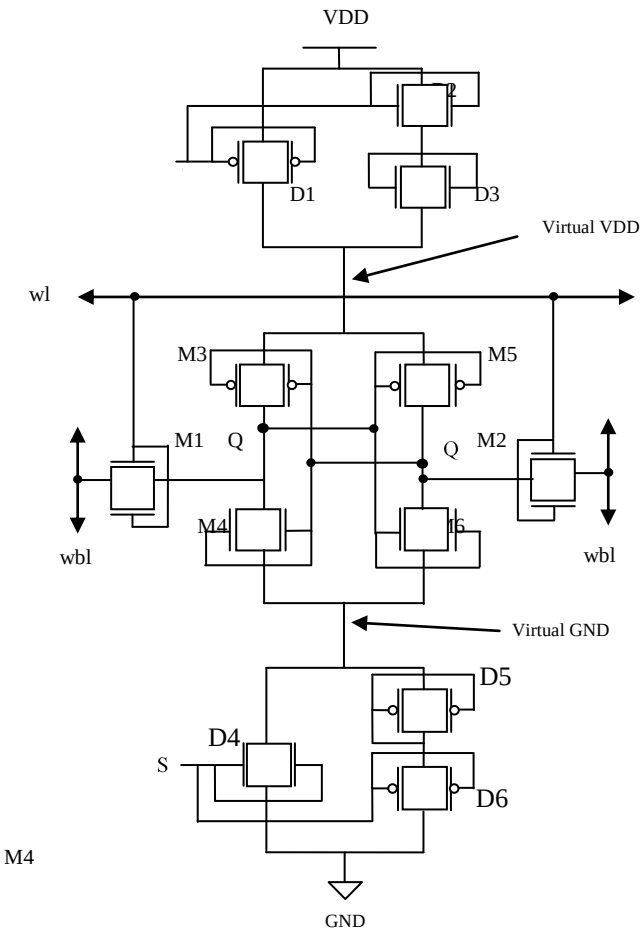

Fig. 8. Implementation of SVL technique on FinFET based 6T SRAM cell

A circuit containing two series NMOS transistors connected in parallel with a PMOS transistor between VDD and 6T FinFET SRAM cell. Another circuit containing two series PMOS transistors connected in parallel with a NMOS transistor between 6T FinFET SRAM cell and GND. Both of these circuits are termed as USVL (upper SVL) and LSVL (lower SVL) respectively which together provides the reduced leakage to the FinFET based 6T SRAM cell [6-8].

As seen in Figure 8, when the circuit is working in active mode, at that time the sleep signal is S= '0' and S□ = '1'. The circuit gets connected with VDD and GND. When the circuit is working in standby mode, at that time the sleep signal is S= '1' and S□ = '0'. So due to series connection of NMOS transistors in the upper SVL, the value of Virtual VDD will be lower as compared to VDD due to voltage drop and due to series connection of PMOS transistors in the lower SVL, the value of Virtual GND will be larger as compared to GND.[9-10] Thus using SVL technique, the overall voltage of the circuit is minimized which results in the reduction of leakage power. Leakage current and Leakage power waveform of FinFET based 6T SRAM implemented using the SVL technique is shown in Figure 9 and Figure 10 respectively.

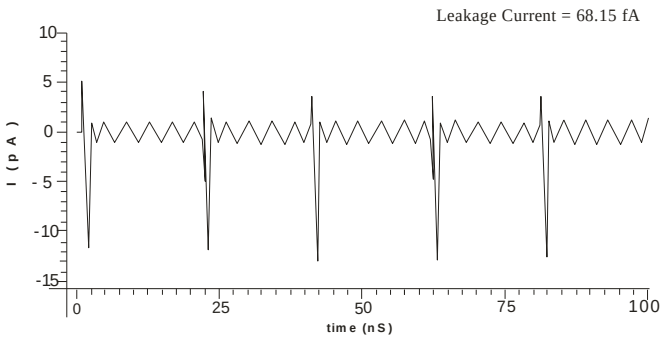

Fig. 9. Leakage current waveform after implementation of the SVL technique on FinFET based 6T SRAM cell

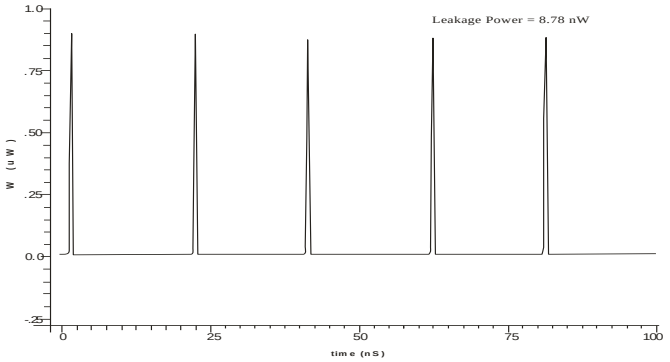

Fig. 10. Leakage power waveform after implementation of the SVL technique on FinFET based 6T SRAM cell

IV CONCLUSION

In this paper, FinFET based 6T SRAM cell has been designed and analysis has been carried out for leakage current and power dissipation. The comparison of the leakage current and power dissipation between the conventional FinFET based 6T SRAM cell and the leakage reduction technique based FinFET based SRAM cells is discussed and shown. Reducing the leakage aspects of the SRAM has been very essential to enhance the stability of the cell. The MTCMOS technique reduces the leakage current and power dissipation by 21.38% and 28.17%. The SVL technique reduces the leakage current and power dissipation by 13.15% and 19.59%. The simulations have been carried out at 45nm technology on cadence virtuoso tool.

ACKNOWLEDGMENT

This work has been done with the help of Cadence Design System Bangalore, India and the author would like to thankful to ITM, Gwalior for providing the tools and technology for the work to be completed. The Author would also like to thank Mrs. Esther Rodriguez Villegas, faculty Imperial College of London for her valuable suggestions time to time.

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