Design and Analysis of Reduce Ground Bounce Noise and Low Leakage Current of Static CMOS Parallel Self Time Adder

Anoop Kumar Singh
M.Tech. Student
Rama University, Kanpur, India
anoop6517@gmail.com
Raghvendra Singh
Assistant Professor
Rama University, Kanpur, India
raghav.raghvendra7@gmail.com

Abstract: High leakage current in deep-sub micrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. This has made power gating techniques an attractive choice for low power applications. But, this introduces ground bounce noise which is also an important challenge. So, low leakage and low ground bounce aware power gating techniques are evaluated in this paper. Techniques such as stacking power gating. Power Gating is one such well known technique where a sleep transistor is added between actual ground rail and circuit ground. The device is turned off during sleep mode to cut-off the leakage path. This technique results in a substantial reduction in leakage at a minimal impact on performance. This paper will focus on reducing sub threshold leakage power consumption and ground bounce noise during the sleep to active mode transition. The adder cells mainly focus on reduction of power and increasing of speed. For mobile applications, designers Work within a limited leakage power Specification in order to meet good battery life. The designers a part from leveling of leakage current to ensure correct circuit operation also focuses on minimization of power dissipation. In the present paper we will propose low leakage 4 bit Parallel Self Time Adder CMOS circuit in 180nm technology with supply voltage of 1V. We will perform analysis and simulation of various parameters such as standby leakage power, active power, ground bounce noise and propagation delay using Cadence aether tool with 180nm standard CMOS technology.

Keywords: Adder cell, Ground bounce noise, Leakage power, stacking power gating, Sleep transistor**.**

1. INTRODUCTION

The leakage current contributes 50-60% in active power [1-2] of digital circuit. One of the most important issues in VLSI design is stand by leakage current with continuous down scaling in advanced CMOS technology. The power reduction must be achieved without trading-off performance which makes it harder to reduce leakage during normal (runtime) operation. Electronic device such as mobile phone is used commonly these days. It's battery life span is of great concern. When mobile phone is operated in standby mode, certain programs of mobile phone are turned off during active or talk mode but this doesn't stop the battery from getting depleted. In this paper, we have proposed new Parallel Self Time Adder with low power and reduce ground bounce noise based on Stacking Power Gating Technique The aim of paper is to implement the full adder to reduce power and to increase speed [3-4]. This techniques uses improvement of power efficiency and ground bounce noise reduction of the A Parallel self Time adder at 180 nm technology. Ground bounce noise [5] – [9], also known as simultaneous switching noise (SSN) or delta-I noise, is a voltage glitch induced at power/ground distribution connections due to switching currents passing through either wire/ substrate inductance or package lead inductance associated with power or ground rails. Ground bounce noise phenomenon during mode transition and leakage current in standby mode is investigated in this paper. We have seen several techniques proposed to reduce leakage power [10]. To decrease the ground bounce noise and leakage power, a modified design with the stacking power gating technique is shown in Fig. (9) and (10). In this technique stack sleep transistor is connected to the virtual ground of the circuits to reduce the magnitude of voltage glitches and current and reduction of leakage power by stacking effect, when both the sleep transistor ST1 and ST2 is turn off (sleep mode). Here with help of select input we have reduced ground bounce noise and this is achieved by the adjusting both the transistor with help of ΔT (delay between the both sleep transistor) (sleep to active mode) [12]. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode [11]. NMOS footer switches can also be used as sleep transistors.

2. Parallel Self Time Adder

The architecture and theory behind PASTA is presented in this section. The adder first accepts two operands to perform half-additions for each bit. Subsequently, it iterates using earlier generated carry and sums to perform half-additions repeatedly until all carry bits are consumed and settled at zero level.

2.1 Architecture of PASTA:

The general block diagram of the Parallel Self-Timed Adder (PASTA) is presented in Fig.1 The selection input for two-input multiplexers corresponds to the Req handshake signal and will be a single 0 to 1 transition denoted by SEL. It will initially Select the actual operands during SEL = 0 and will switch to feedback/carry paths for subsequent iterations using SEL = 1. The feedback path from the HAs enables the multiple iterations to continue until the completion when all carry signals will assume zero. The sequential circuits are often serial/chain adders and are not the match for high speed combination adder. Multi bit adders are often constructed from single bit adders using combinational and sequential circuits for asynchronous or synchronous design.

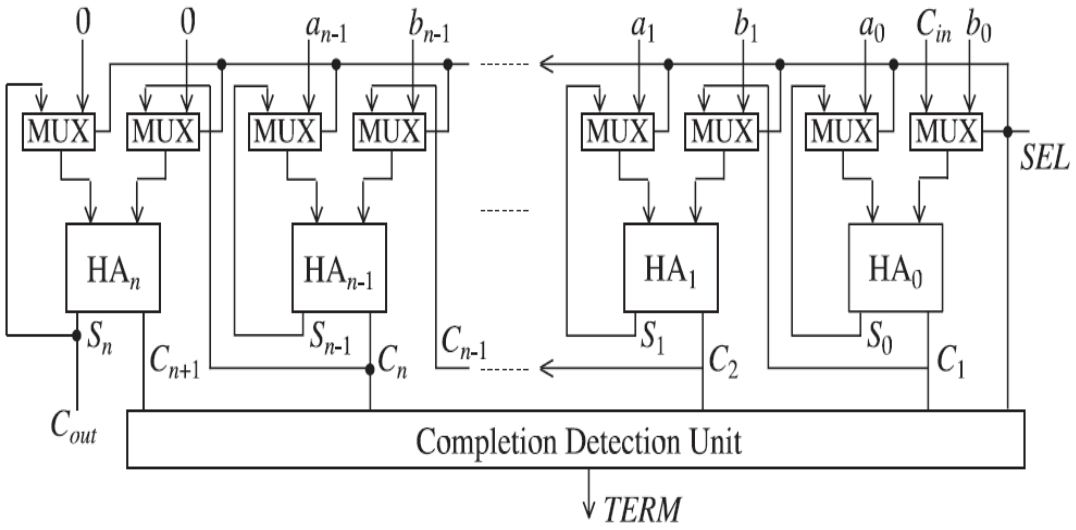
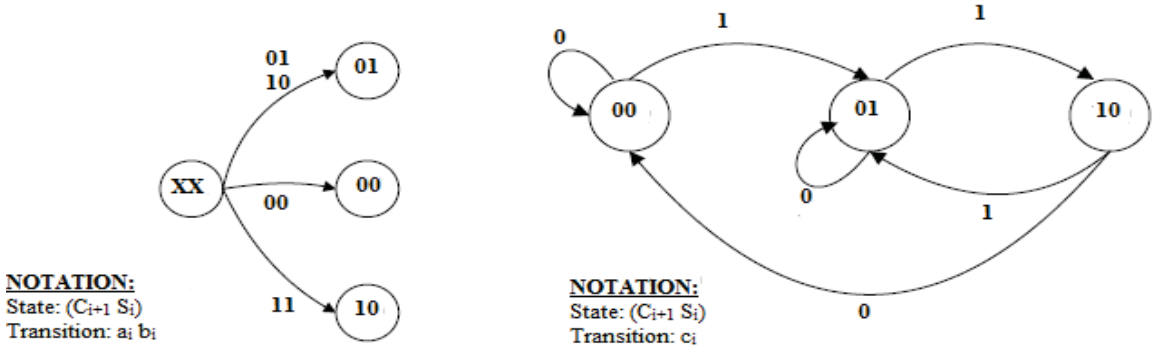


Fig1. Parallel Self Time Adder

2.2 State Diagram:

In Fig. 2, two state diagrams are drawn for the initial phase and the iterative phase of the proposed architecture. Each state is represented by (*Ci*+1, *Si*) pair where *Ci*+1, *Si* represent carry out and sum values, respectively, from the i^{th} bit adder block. During the initial phase, the circuit merely works as a combinational HA operating in fundamental mode. It is apparent that due to the use of HAs instead of FAs, state (11) cannot appear. During the iterative phase (SEL = 1), the feedback path through multiplexer block is activated. The carry transitions (*Ci*) are allowed as many times as needed to complete the recursion.



(a) Initial phase (b) Iterative Phase

Figure 2: Initial and Iterative Phase State Diagrams for PASTA

2.3. Implementation of Parallel Self-Timed Adder (PASTA):

A CMOS implementation for the recursive circuit is shown in Fig. 3. For multiplexers and AND gates we have used TSMC library implementations while for the XOR gate we have used the faster ten transistor implementation based on transmission gate XOR to match the delay with AND gates [15]. An alternative more practical pseudo-nMOS ratio-ed design is used. This requires a large fan-in *n*-input NOR gate. The resulting design is shown in Fig. 3(d). The pMOS transistor connected to *V*DD of this ratio-ed design act as a load register, resulting in static current drain when some of the nMOS transistors are on simultaneously. the pseudo-nMOS design, the completion unit avoids the high fan-in problem as all the connections are parallel. The negative of SEL signal included the term signal. During the initial selection phase of the actual inputs. It is ensure that the completion can not be accidently turned on. The PMOS Pull up Transistor always on, during the duration of the actual computation a static current will flow.

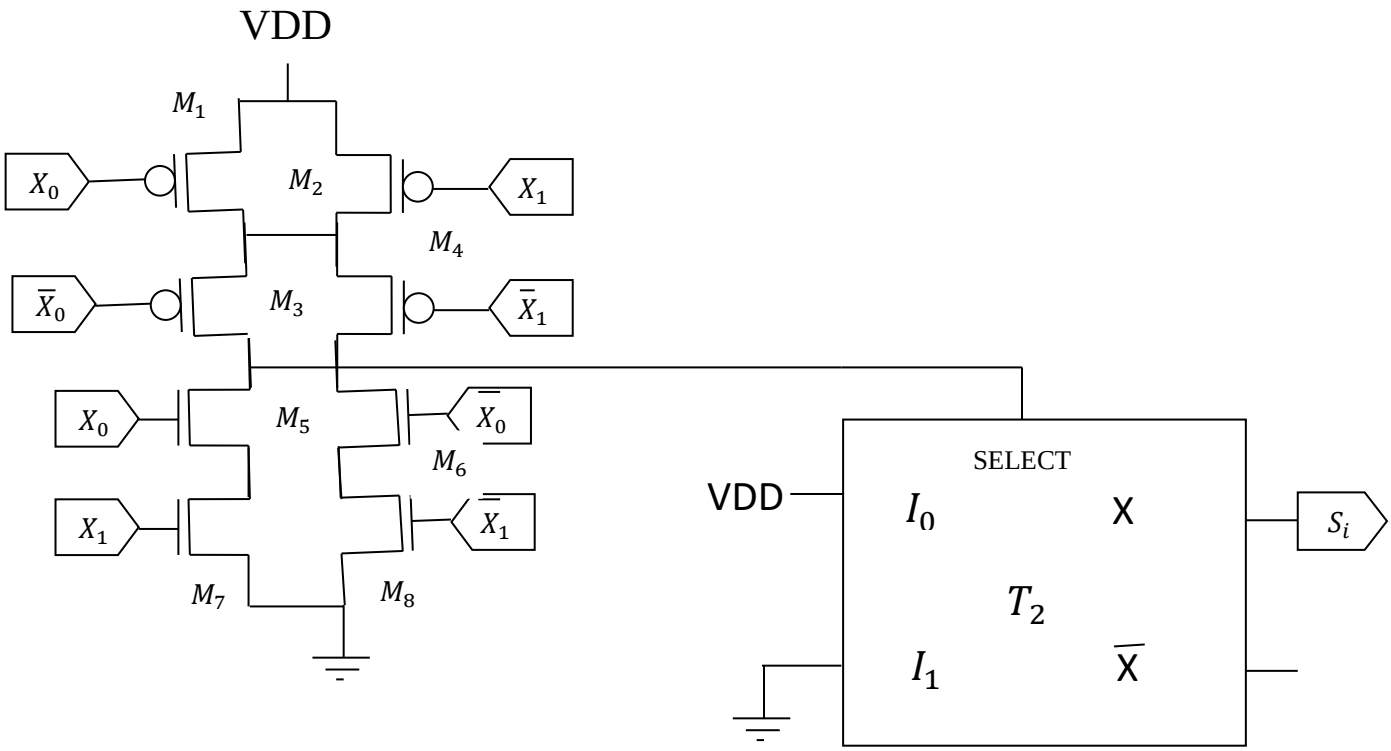


Fig.3

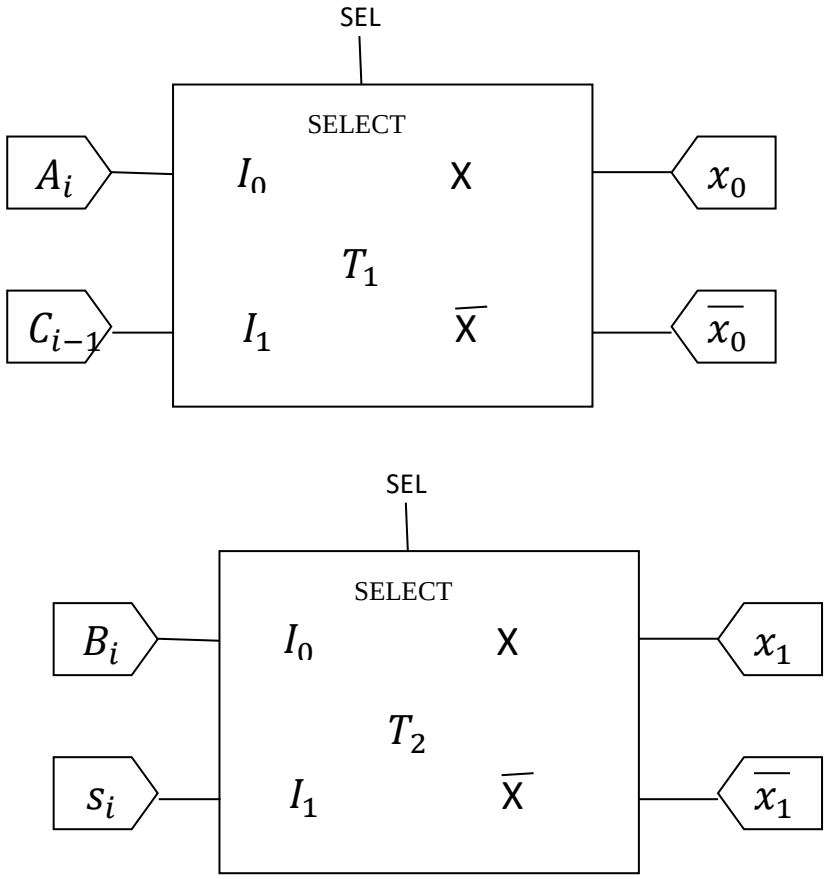


Fig.5

A Single bit Adder module in (fig 3, fig 4, fig 5).

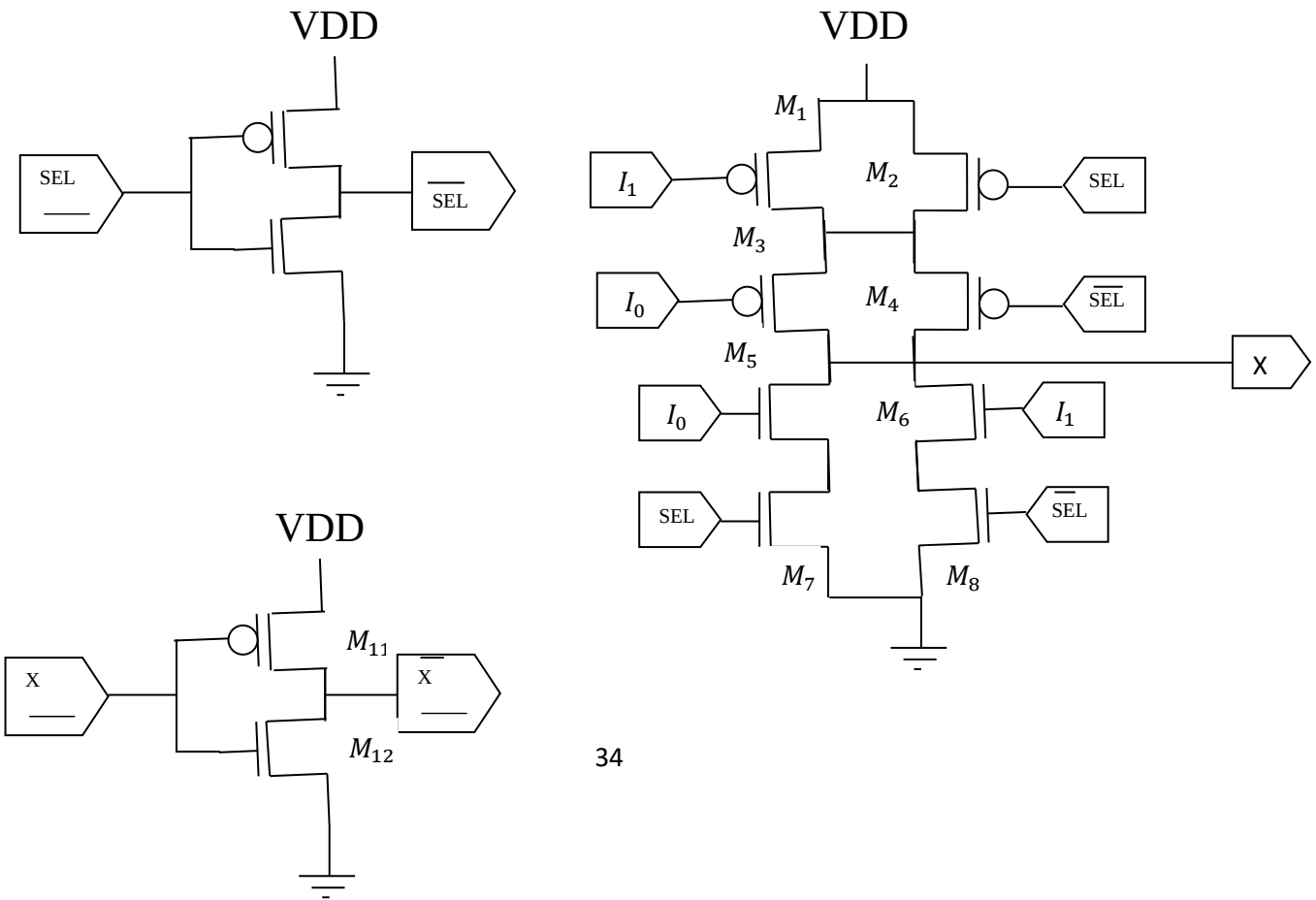


Fig.6. (2×1 MUX for 1 Bit Adder)

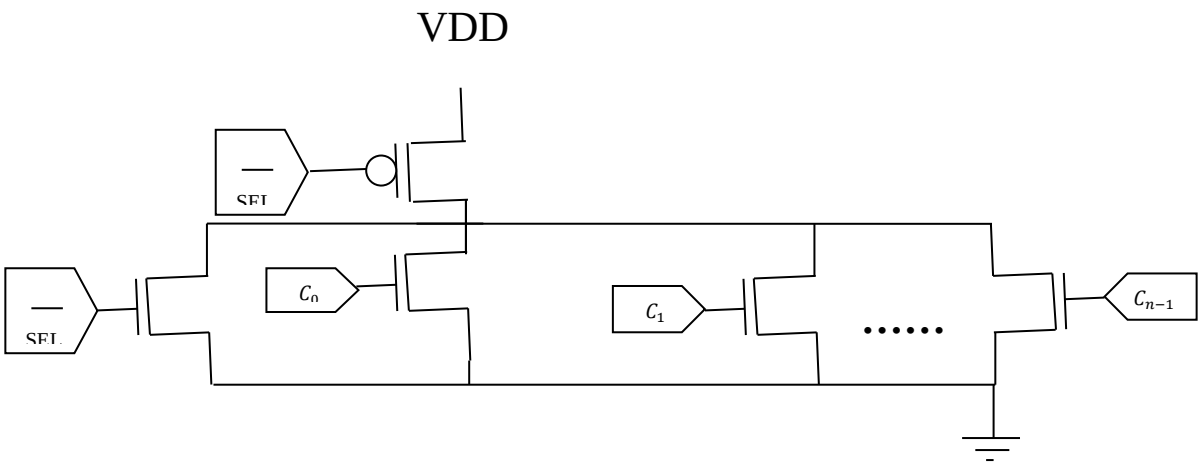


Fig.7.(The Termination signal generation circuit)

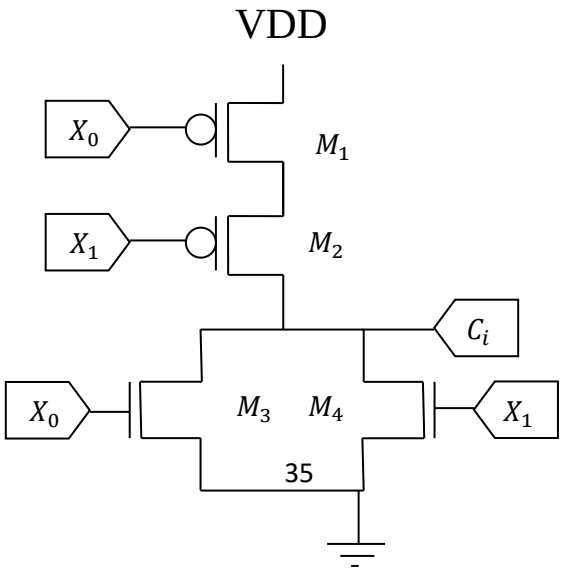


Fig.8. (A Signal Bit carry module)

In this technique, both MSL1 and MSL2 sleep transistors are turned off. Here, SELECT input is applied in such a manner that ground bounce noise is lowest and this is achieved by keeping the value of ΔT which gives the summation of ground bounce noises of these two transistors lowest. If ΔT is half the oscillation period of the ground bounce noise then the positive peak of the ground bounce noise lay over the negative peak there by bringing ground bounce noise closer to zero. In this technique we used the stacking sleep transistor to minimize the peak current and voltage glitches in power rails i.e ground bounce.

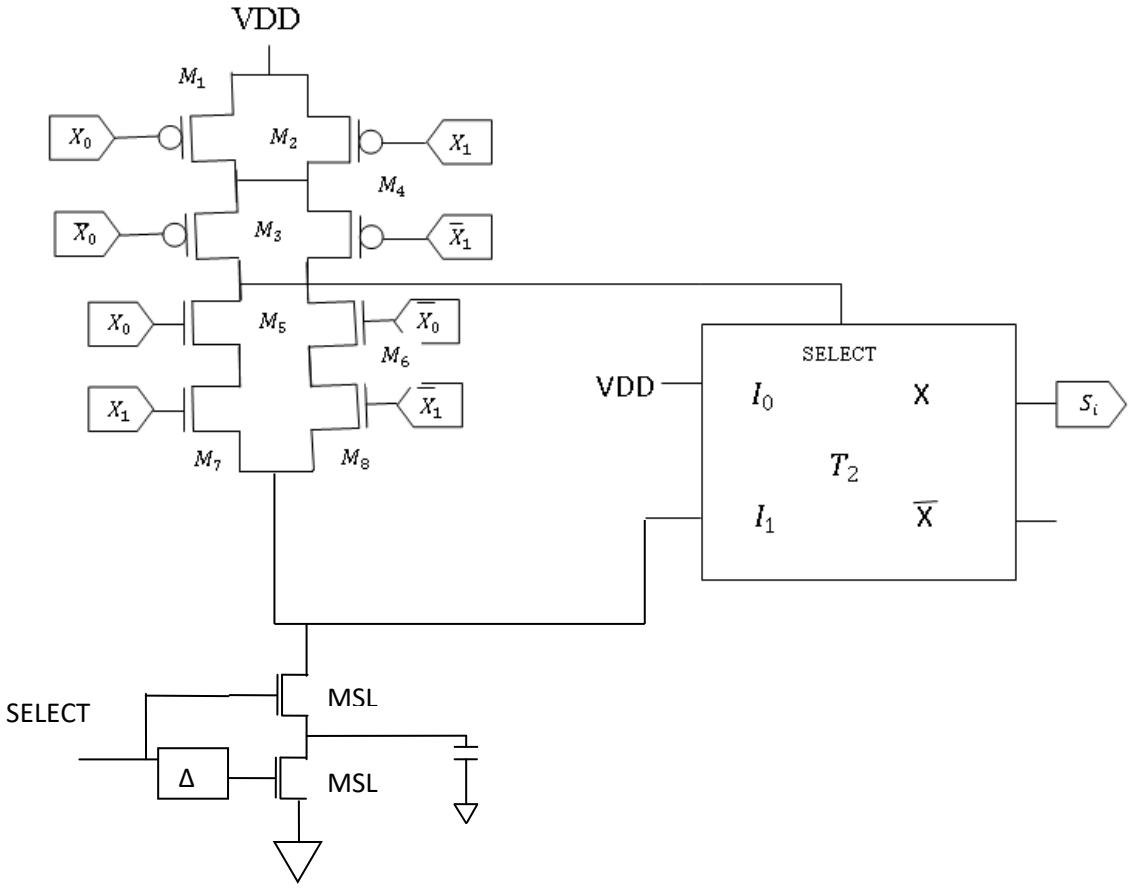


Fig.9.Modified 4 bit A Parallel self time Adder with forward body biased Stacking Power Gating Technique.

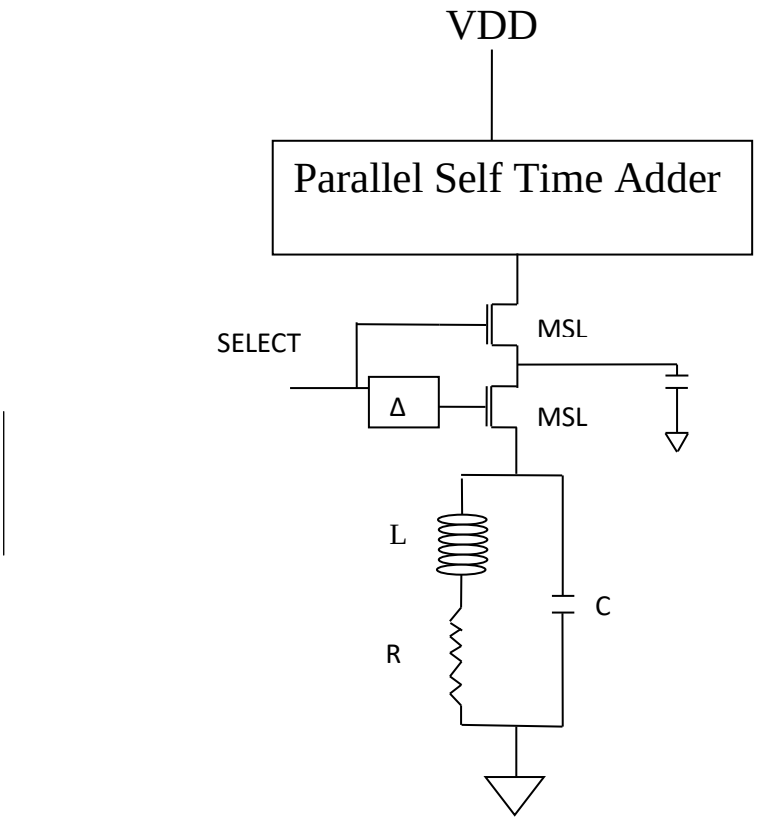


Fig.10.Modified 4 bit A Parallel self time Adder with forward body biased Stacking Power Gating Technique and ground bounce noise.

3. PERFORMANCE ANALYSIS AND SIMULATION

In this section, we have performed simulation of our base structure PASTA and modified PASTA adder (adder with FBB Stacking Power Gating Technique) on Cadence aether Tool and SPECTRE Simulator at 180 nm Technology.

3.1. Active Power:

The Active power is dissipated by the circuit when the circuit is operation state. Here we will calculate the active power of circuit on the basis of voltage and temperature at 180 nm technology. The Active power includes both dynamics and static power. The Active power consumption of CMOS circuit [17] [18] is described by the following equation.

$$P_{active} = P_{dynamic} + P_{static} \quad (1)$$

$$P_{active} = P_{switch} + P_{short} + P_{leak} \quad (2)$$

$$P = \alpha_{0\to1} \times C_1 \times F_{clock} \times V_{dd}^2 + I_{short-circuit} \times V_{dd} + I_{leakage} \times V_{dd} \quad (3)$$

Where, $\alpha_{0\,to1}$= probability, C_1=load capacitance,F_c =Clock Frequecy, Vdd=power supply, I_{short} =short circuit current, I_{leak} =leakage current As shown the table 1. figure(9) and (10) in the case of modified 4 bit a Parallel self time adder with forward body biased multimode MTCMOS active power is reduced compared to conventional A Parallel self time adder .The reduction almost 57.71 % at voltage 0.7 V and temperature 27^0 C.

Table 1: Active Power

Circuit	Base Pasta Adder		Modified Pasta Adder	
Supply and Temperature	.7v	27℃	.7v	27℃
Active power	112.75	112.75	48.89	48.89

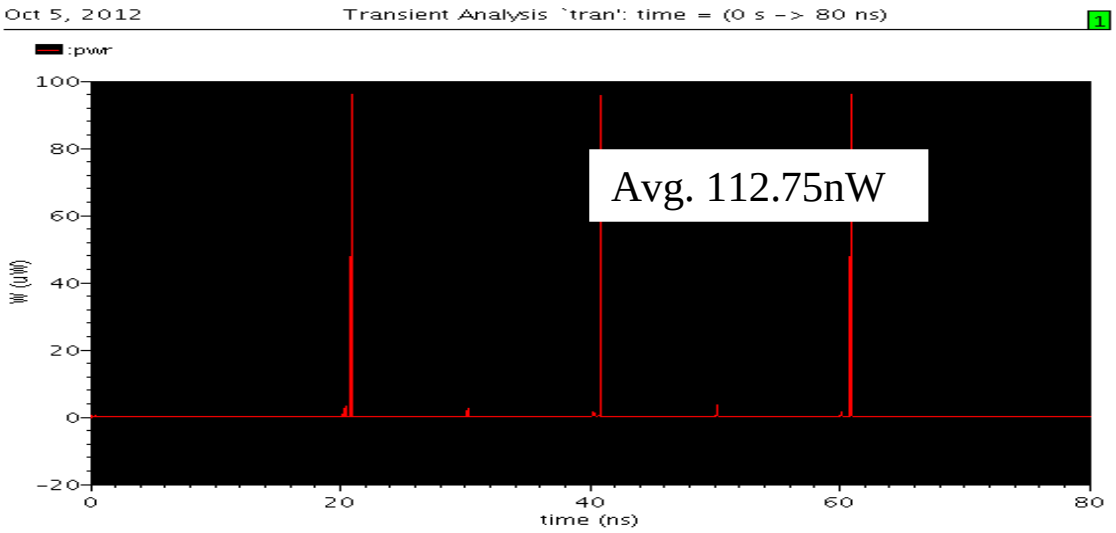


Fig.11.Active Power of conventional 4 bit PASTA

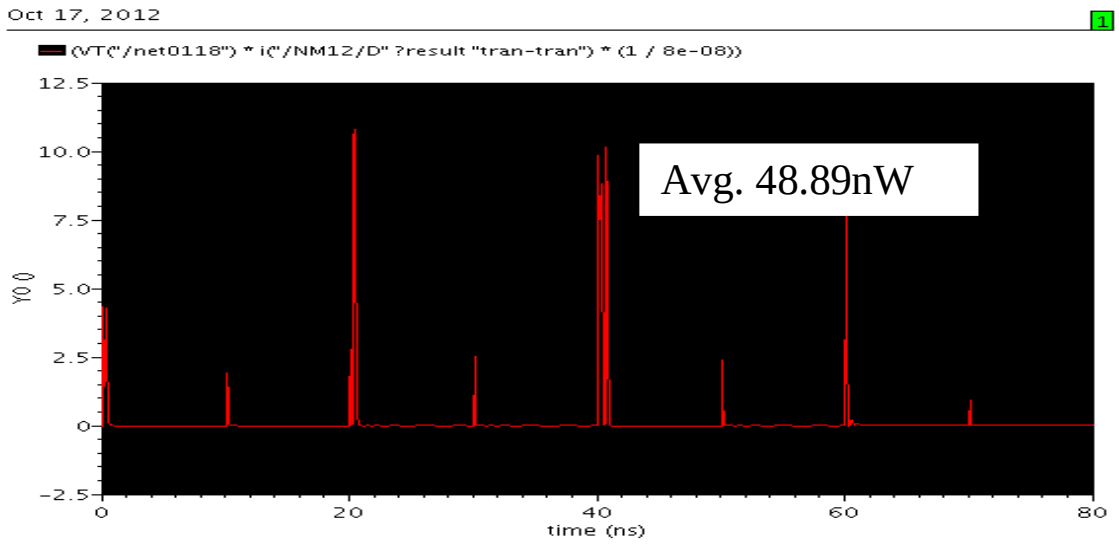


Fig.12.Active Power of Modified 4 bit PASTA

3.2. Stand By Leakage Current:

The stand by leakage is obtained when the circuit is in idle mode. When the leakage current measures in stacking power gating then both transistors are off [21]. Here the sleep transistor connects to the pull down network of Parallel self time adder circuit and ground of the circuit. The basic equation of stand by leakage

$$I_{leakage} = I_{sub} + I_{ox} \quad (4)$$

$$I_{sub} = K_1 W e^{-Vth/nV_0} \left[1 - e^{-\frac{V}{V_0}}\right] \quad (5)$$

Where, I_{sub} = threshold leakage current I_{ox}= Gate oxide current.

Where k1 and n is experimentally derived, W is gate width, Vθ is thermal voltage, n slope shape factor/ sub threshold swing coefficient, V_{th} is threshold voltage.

$$I_{ox} = K_2 W [\frac{V}{T_{ox}}]^2 e^{-\alpha T_{ox}/V_0} \quad (6)$$

Where K_2 and α are experimentally derived, Tox is oxide thickness.

Stand by leakage current is measured by at 0.7V and 27℃. It is greatly reduced almost to 90% in modified Parallel Self Time adder with stacking power gating. The table 3, 4 and figure 13 and 14 shows the leakage current at various voltages and various temperatures.

Table 2: Stand by Leakage current and leakage power due to various voltages

Volt(v)	Leakage Current		Leakage Power	
	Base Pasta (nA)	Modified Pasta (PA)	Base Pasta (nw)	Modified Pasta (pw)
0.5	94.65	49.67	32.61	103.76
0.7	161.43	81.92	73.68	116.30
0.9	233.49	160.45	146.71	136.13
1.1	284.65	221.20	294.32	146.33
1.3	378.78	402.44	349.32	227.53

Table 3: Stand by Leakage current and leakage power due to various temperatures

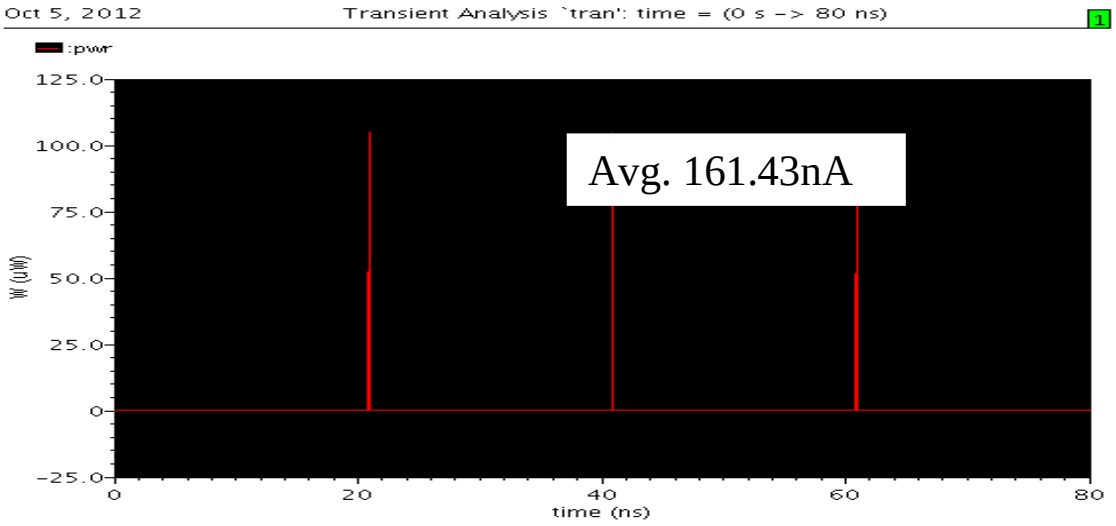
Temp.℃	Leakage Current		Leakage Power	
	Base Pasta (nA)	Modified Pasta (PA)	Base Pasta (nw)	Modified Pasta (pw)
27	161.63	81.65	73.43	116.43
47	163.32	142.53	179.54	258.60
67	165.31	252.71	81.54	390.26
87	168.55	322.21	83.54	446.62
107	196.23	428.01	93.09	574.16

3.3. Stand by leakage Power:

Basically the standby leakage power is the product of the leakage current and supply voltage [20]. Here when the sleep transistor is off, we measure the leakage power. The stand by leakage power is measured at the time of idle mode. The basic equation of leakage power is

$$P_{leakage} = I_{leakage} \times V_{dd} \quad (7)$$

Where Vdd=Power supply, $I_{leakage}$ =Leakage current, P_{leak} = Leakage power. The table (3) (4) and figure 15,and 16 show that leakage power is reduced in various voltages and temperatures after applying stacking power gating. This basic concept would be utilized to improve the power performance of the adder in this paper. Lowering Vdd would significantly reduce the power consumption of the circuit. The equation shows that the power depends on different parameters as well as on supply voltage (Vdd).



. **Fig.13. Leakage Current of conventional 4 bit PASTA**

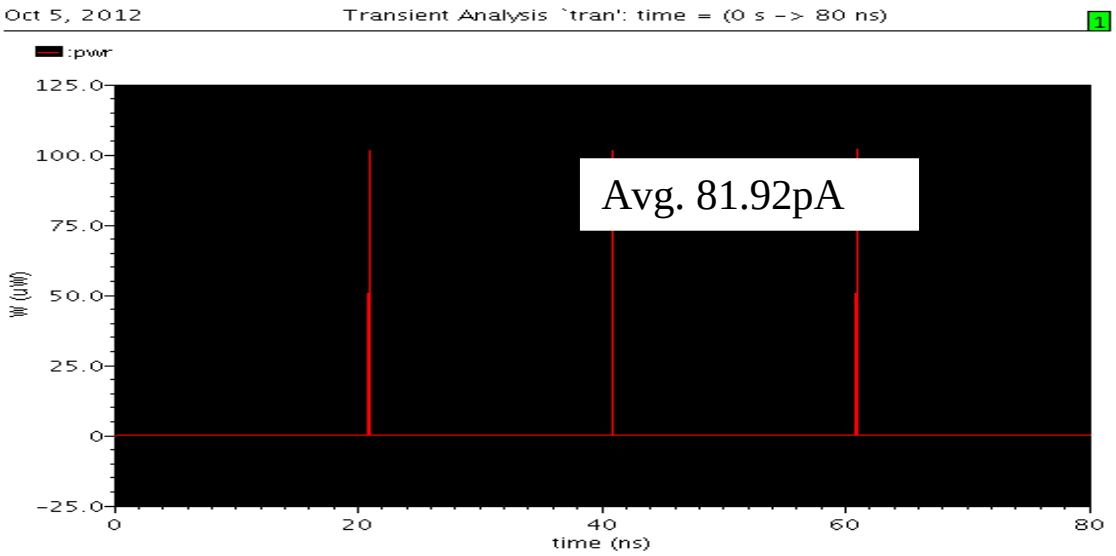


Fig.14.Leakage Current of modified 4 bit PASTA

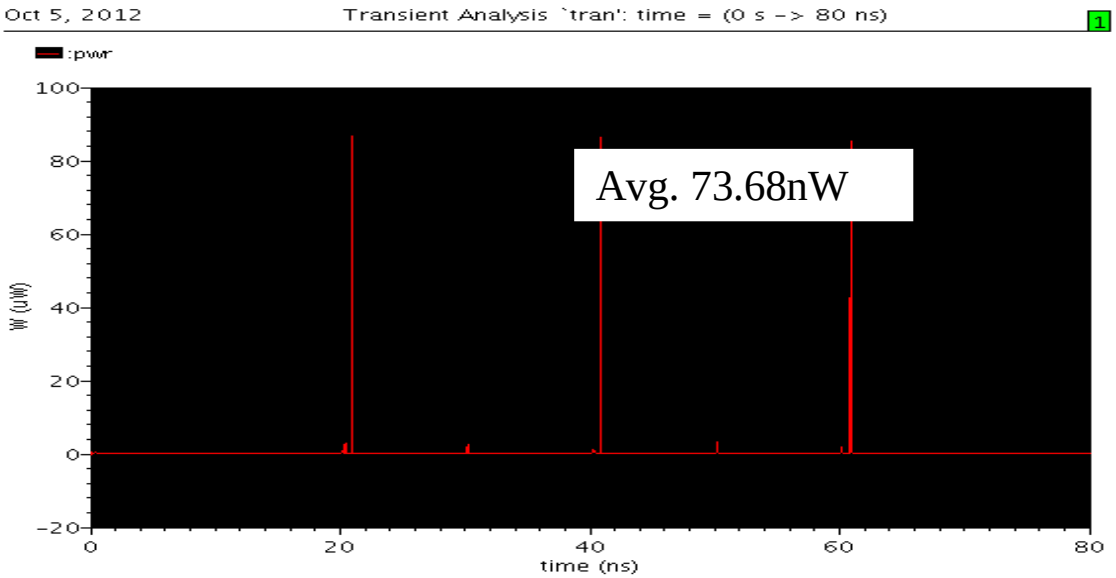


Fig.15.Leakage power wave of conventional 4 bit PASTA

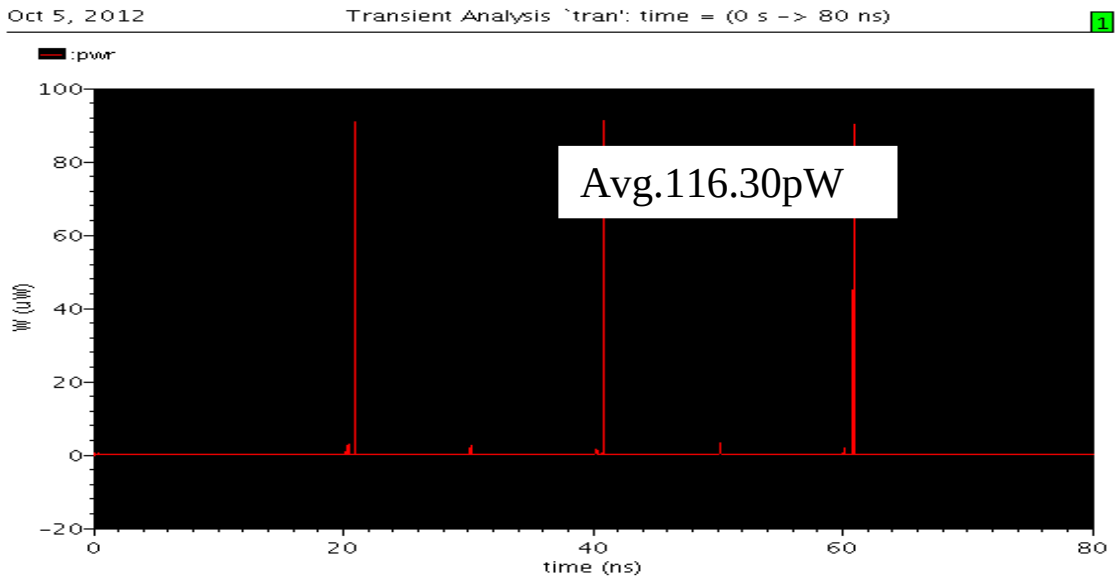


Fig.16.Leakage power wave of modified 4 bit PASTA

3.4. Ground Bounce Noise:

There are some methods such as power gating to address the problem of ground bounce in low-voltage CMOS circuits. All the designs we are reduced the ground bounce noise using the Stacking power gating logic circuits. Ground Bounce is a voltage oscillation between the ground pin on a component package and the ground reference level on the component die. Essentially it is caused by a current surge passing through the lead inductance of the package. The effect is most pronounced when all outputs switch simultaneously. In saturation region an instantaneous charge current passes through the sleep transistor, during power mode transition. The noise depends on the voltage. The ground bounce noise model is shown in Fig (17) and (18)[22]. As shown in the table 4, and figure 19 and 20 the ground bounce noise is reduced up to 55 % in to various voltage and temperature.

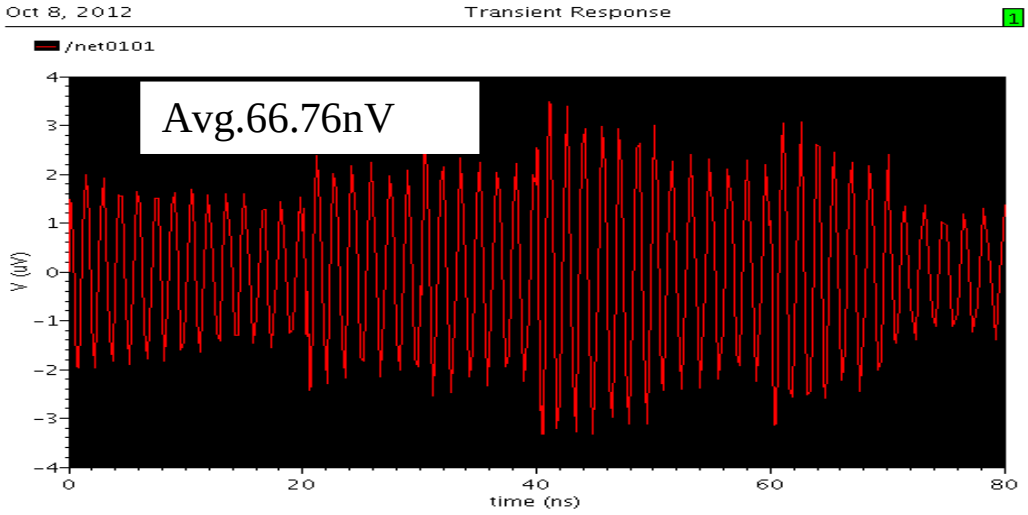


Fig.17.Ground bounce noise of base PASTA

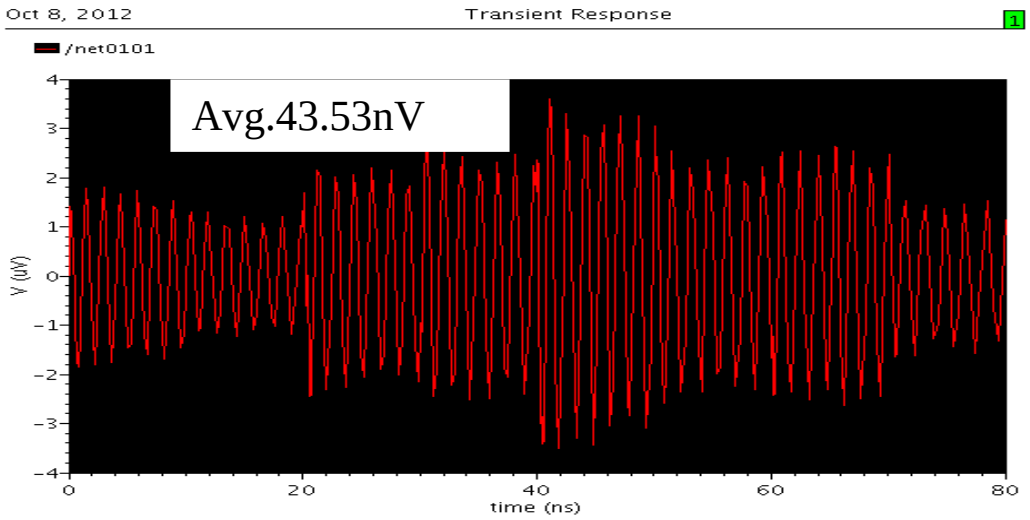


Fig.18.Ground bounce noise of modified PASTA

Table 4 GROUND BOUNCE NOISE OF 4 BITS PARALLEL SELF TIME ADDER

Voltage(v)	Ground Bounce Noise (nv)		Temp.℃	Ground Bounce Noise (nv)	
	Base Pasta	Modified Pasta		Base Pasta	Modified Pasta
0.5	69.54	21.43	27	66.43	43.78
0.7	66.76	43.53	47	69.90	36.64
0.9	99.21	67.36	67	72.21	47.26
1.1	128.86	92.26	87	77.71	56.18
1.3	160.17	118.72	107	83.48	66.66

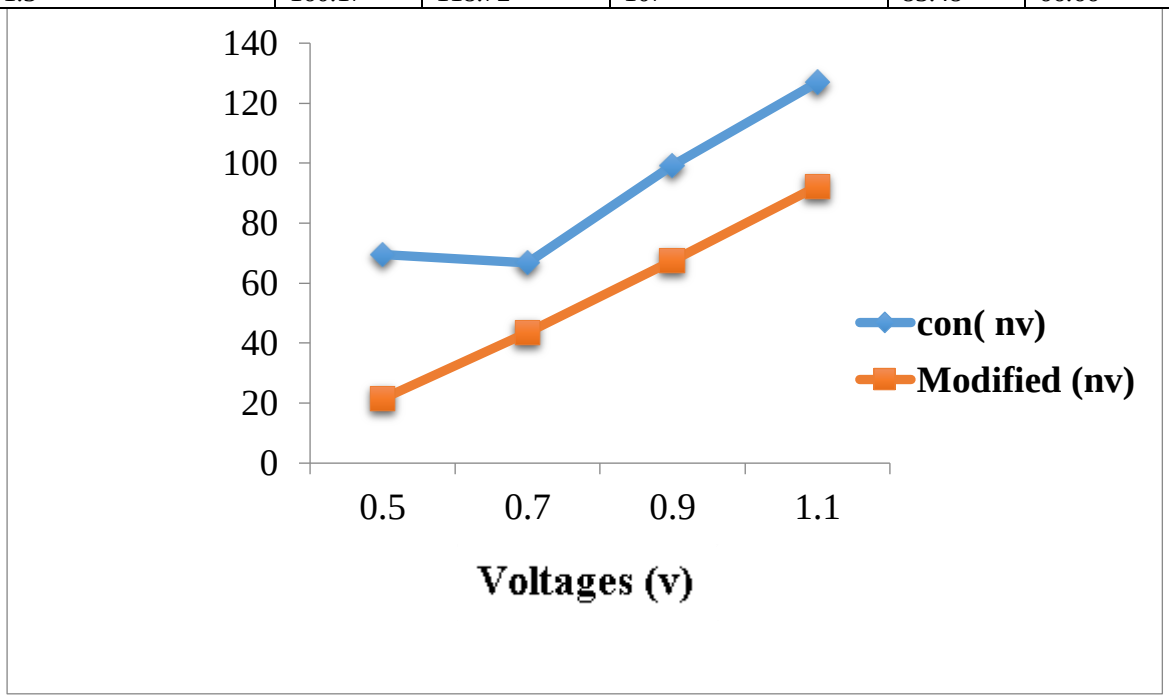


Fig.19.Ground Bounce Noise graph of PASTA at various voltage

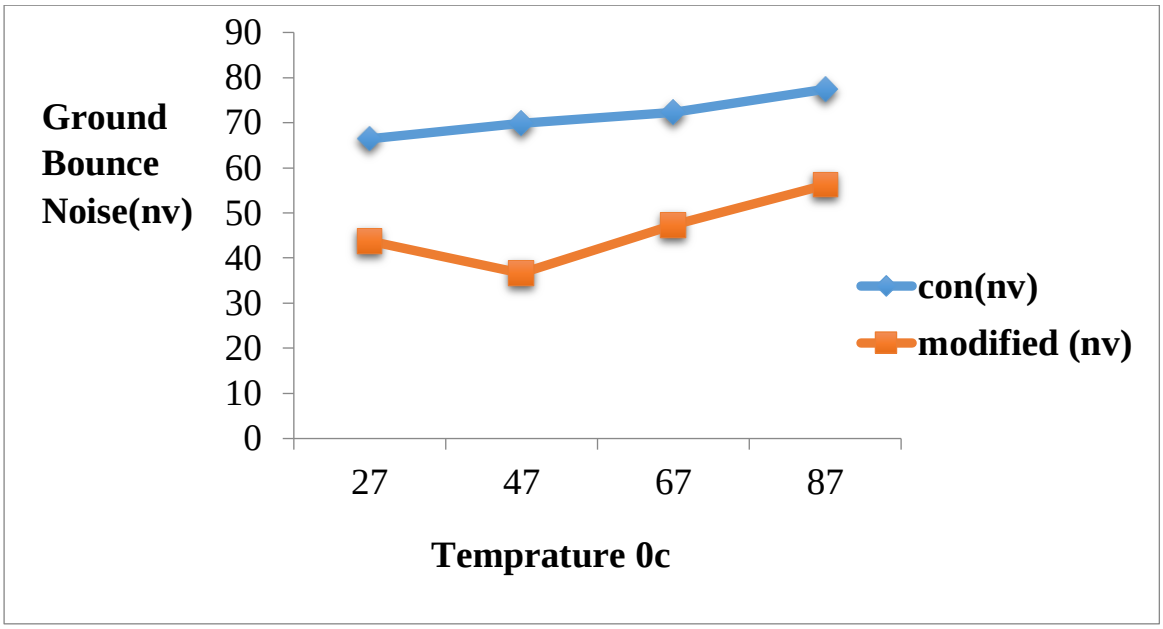


Fig.20.Ground Bounce Noise graph of PASTA at various Temprature

Conclusion:

Standby leakage current, ground bounce noise and power consumption for stacking power gating, approaches is evaluated in this paper. and successfully reduces ground bounce noise, stand by leakage current with considerable amount. Effect of temperature on ground bounce noise and standby leakage current for different power gating approaches for high speed 4- bit parallel self time adder circuit have been also analyzed in this paper.

A stacking power gating approach has been presented which reduces peak of ground bounce noise, standby leakage current and active power dissipation. It has been evaluated that this approach reduces standby leakage current by 89.8% and active power by 80.06% . The reduction of ground bounce noise is also considerable in this approach. Ground bounce noise is also evaluated with temperature variations. Sleep transistors are kept at high threshold voltage to reduce the standby leakage current. This technique reduces the standby leakage current and active power by 96.5%, 94.95% respectively as on compared to conventional mode.

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